University of Alberta

Experimental Validation of a Flatness-based Control for a Voltage Source Converter

by

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Abstract

A voltage source converter (VSC) is a power electronic device used in many applications including wind turbine generators, induction motor drives, and power transmission and delivery. This thesis develops a high performance control for a 3-phase 6-pulse IGBT-based VSC intended for power transmission and delivery applications. The industrial standard for VSC control is a Proportional-Integral (PI) control scheme based on a linear approximate system model. Since it is based on a linear approximate model, only local performance is ensured. In order to provide performance over a range of operating conditions this thesis proposes a nonlinear flatness-based control which avoids the linearization step. A full experimental validation of the proposed control is given. This thesis involves a collaborative effort between the Applied Nonlinear Control Laboratory (ANCL) and the Real-Time eXperimental LABoratory (RTX-LAB) at the University of Alberta.

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Chapter 1

Introduction

Power converters have been utilized in various applications over a broad range of industry. For example, AC machines such as induction motors and permanent magnet synchronous machines (PMSMs) require voltage conversion, either a DC-AC conversion or an AC-DC-AC conversion with proper magnitude and frequency in order to drive the machines in a desired manner. Electric power generators such as wind turbines also require converters in order to transform the generated energy into usable electric power. In power transmission and delivery, converters play an important role in optimization of power flow in AC power transmission systems. Hence, the control of these converters has become an important issue as well as an active research topic in power systems. Many types of converters exist; in this thesis we focus on the 3-phase 6-pulse Voltage Source Converter (VSC). The basic function of the VSC is an AC-DC bi-directional voltage conversion. However in power systems applications, the VSC acts either as a controlled current source or as a controlled voltage source (depending on its connection to the power line) and hence, a VSC can function as a power flow controller [12].

The variety of applications of power converters have been made possible due to recent development and improvement in power electronic semiconductor devices that are capable of handling high power, faster switching and low power loss. These switching devices contained in the VSCs are responsible for performing power conversion and therefore, efficient control technique of the switches are crucial in obtaining a desired performance. The industry

standard control technique for the VSCs is the conventional Proportional-Integral (PI) control. The motivation for this thesis is the development of advanced control techniques to investigate whether the performance of the VSC can be improved.

This thesis involves a collaborative effort between the Applied Nonlinear Control Laboratory (ANCL) and the Real-Time eXperimental LABoratory (RTX-LAB) at the University of Alberta to develop a high performance nonlinear control for a 3-phase 6-pulse IGBT-based VSC intended for power transmission system applications. In the following section, we provide specific examples of power transmission systems which rely on VSCs.

1.1 Applications of VSC in Power Transmission and Delivery

Power electronic devices such as VSCs can be used to optimize power transfer capability and minimize power loss in AC Transmission lines. A transmission system where such devices are used to provide the needed corrections of transmission characteristics are known as Flexible AC Transmission Systems (FACTS) [7]. In other words, FACTS is a system that contains a power flow controller in the AC transmission systems in order to optimize power transfer. In this section we discuss how VSCs are used to control power flow in AC transmission systems and also look at two types of FACTS technologies; a Unified Power Flow Controller (UPFC) and a Static Compensator (STATCOM).

1.1.1 Power Flow in Transmission Lines

We begin with mathematical representations of real and reactive power in transmission lines. See [11] for a detailed discussion on power flow and transmissions. Figure 1.1 shows a simple AC transmission line with sending-end voltage phasor $\mathbf{V_S} = |V|e^{j\theta}$, receiving-end voltage phasor $\mathbf{V_R} = |V|e^{j(\theta+\delta)}$, and line impedance X. The line is assumed purely inductive for simplicity. In Figure 1.2 the corresponding phasor diagram is shown where the transmission angle between the sending-end and the receiving-end is δ and $\mathbf{V_X}$ represents

the voltage drop across the line. The transmitted real power P and reactive

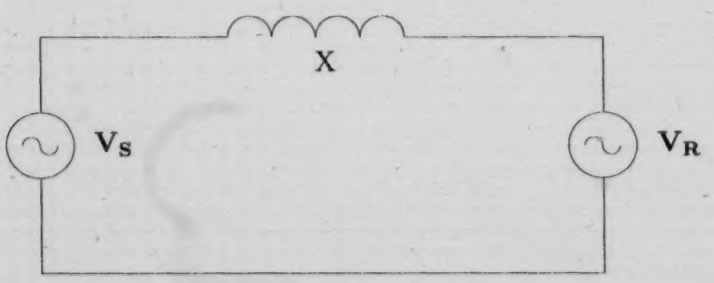


Figure 1.1: Simple transmission system

power Q can be expressed by

$$P = \frac{V^2}{X}\sin\delta, \quad Q = \frac{V^2}{X}(1-\cos\delta).$$

The real and reactive power flow in the transmission line is governed by the line impedance X, voltage magnitude $|V|$, and the angle difference δ between the line ends [7]. Hence, power flow control involves varying V and δ in order to adjust P and Q.

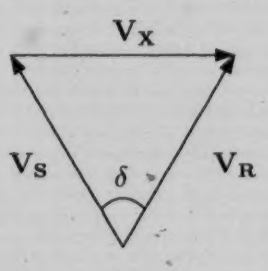


Figure 1.2: Phasor diagram of the sending-end and receiving-end voltages

Now consider Figure 1.3 where a controllable voltage source $\mathbf{V_{pq}}$ is connected in series with the line. This source provides a series voltage injection. By injecting an AC voltage to the line whose magnitude and phase angle can both be controlled, it regulates both the transmitted real and reactive power flow in the transmission line. This approach to power flow control is called *series compensation*. The variable $\mathbf{V_o}$ denotes the voltage before compensation and $\mathbf{V_o'}$ denotes the voltage after compensation. Figure 1.4 (a) illustrates

that the magnitude and the phase angle of $\mathbf{V_{pq}}$ can be controlled within the circular region. Three specific approaches to series compensation are discussed next.

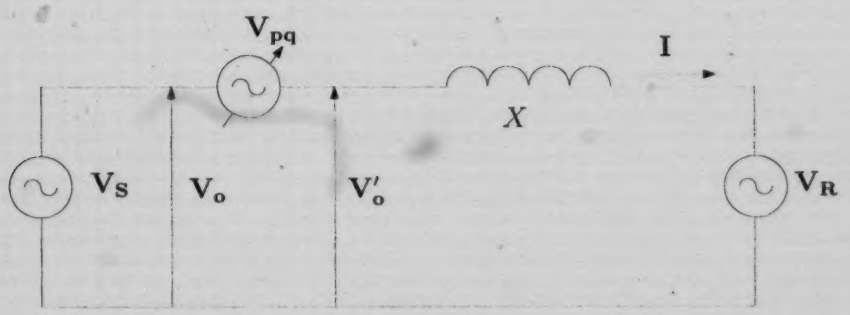


Figure 1.3: Series compensation of a line

1. **Terminal Voltage Regulation:** The sending-end terminal voltage regulation can be obtained by keeping the angle of $\mathbf{V_{pq}}$ in phase with that of $\mathbf{V_o}$ thereby changing only the magnitude of $\mathbf{V_o}$ as shown in Figure 1.4 (b).

2. **Series Capacitive Compensation:** Suppose there exists a capacitive component in series with the line impedance. This creates a phase shift and change in magnitude in the terminal voltage $\mathbf{V_o}$. This shift of $\mathbf{V_o}$ is in the direction perpendicular to $\mathbf{I}$. To compensate for this unwanted phase and magnitude changes, the power flow controller injects a voltage $\mathbf{V_{pq}} = -\mathbf{V_c}$, where $\mathbf{V_c}$ is the voltage phasor caused by the capacitance. See Figure 1.4 (c).

3. **Phase Angle Regulation:** The phase angle control of the terminal voltage can be performed by defining V_{pq} as

$$\mathbf{V_{pq}} = 2V_o \sin\frac{\alpha}{2} e^{j\left(\frac{\pi}{2}-\frac{\alpha}{2}\right)}$$

This implies that the phase angle between V_o and V'_o is changed by α but the magnitude of the voltage remains unchanged as shown in Figure 1.4 (d).

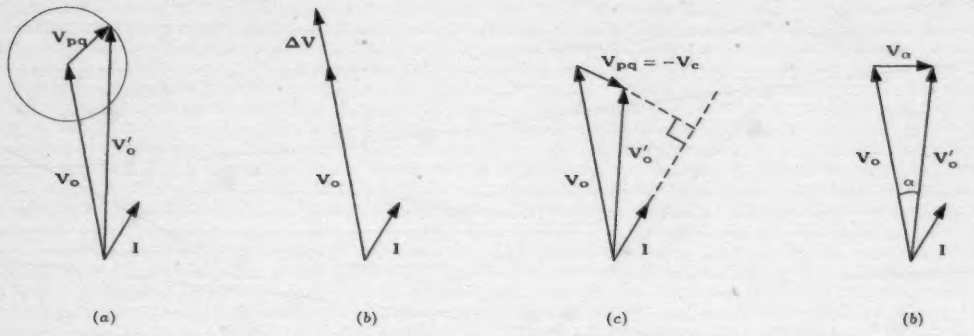


Figure 1.4: Phasor diagram of the series compensation

1.1.2 Unified Power Flow Controller (UPFC)

The power flow control discussed in the previous section is implemented in practice by a UPFC. Figure 1.5 shows the circuit diagram of the UPFC which consists of two 6-pulse VSCs where VSC-1 is connected in shunt with the transmission line through the shunt transformer and VSC-2 is connected to the line through the series transformer. The main function of VSC-2 is the injection of the voltage $\mathbf{V_{pq}}$ to the line with controllable magnitude and phase angle, and hence VSC-2 is responsible for series compensation of the transmission line. The main function of VSC-1 is to supply or absorb the real power demanded by VSC-2. Since VSC-1 is connected in shunt with the line, the UPFC is also able to perform shunt compensation (current injection to the line) and this is discussed in the STATCOM section. Since both converters have a common DC link, this topology can effectively function as an AC-DC-AC power conversion where the real power can flow in both directions and each converter can independently generate or absorb reactive power at the AC terminal.

1.1.3 Static Compensator (STATCOM)

Another application where VSCs are used in power systems is the distribution-static synchronous compensator (D-STATCOM or simply STATCOM) [11]. A STATCOM can be considered as the shunt component (VSC-1) of the UPFC and its main function is to provide power factor correction in the transmission

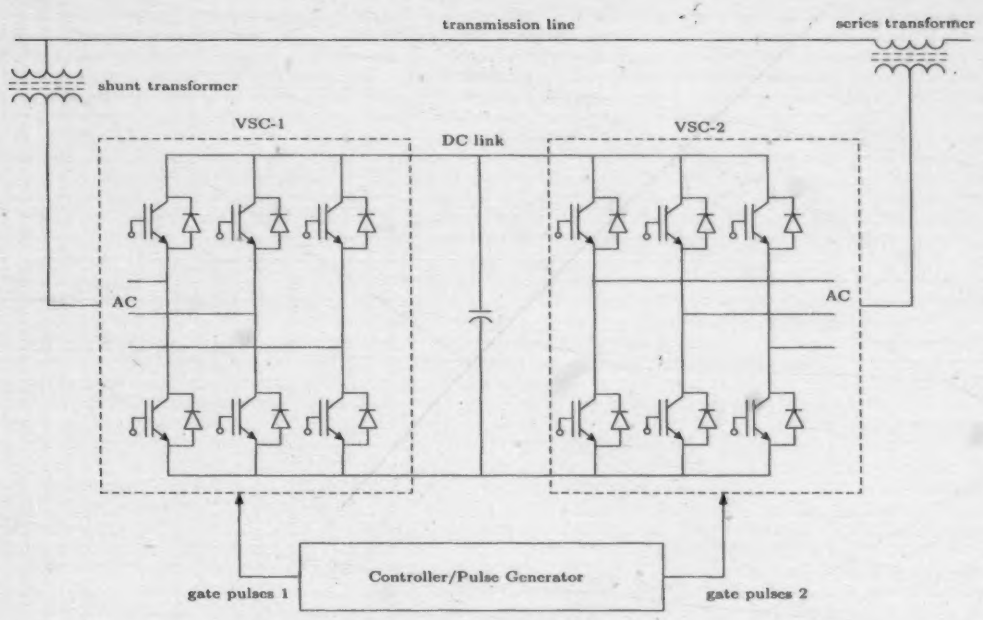


Figure 1.5: Basic circuit diagram of the UPFC

line by regulating the reactive power; it either draws or supplies reactive current which influences the power factor of the line. STATCOM also draws real power in order to charge the DC capacitor, and the energy stored in the capacitor is used to supply the reactive power to the line. Therefore in a STATCOM setup, controlling the DC capacitor voltage and the reactive current of the VSC is the main control objective. Figure 1.6 shows a simple circuit diagram of the STATCOM system where v_S is the power source (power distributor) and R_L and L_L are the loads added by the power users. Having a large inductive load results in poor power factor which leads to power loss and low efficiency of power delivery for the utility company. In order to compensate for this low power factor, a STATCOM is connected in shunt with the distribution line so that the power factor can be corrected by absorbing or supplying the necessary reactive power. Since the VSC contains switching devices, filter inductors L_s are inserted in between to filter out the higher order harmonic components of the voltage.

Figure 1.7 shows the simple circuit and the phasor diagram to illustrate

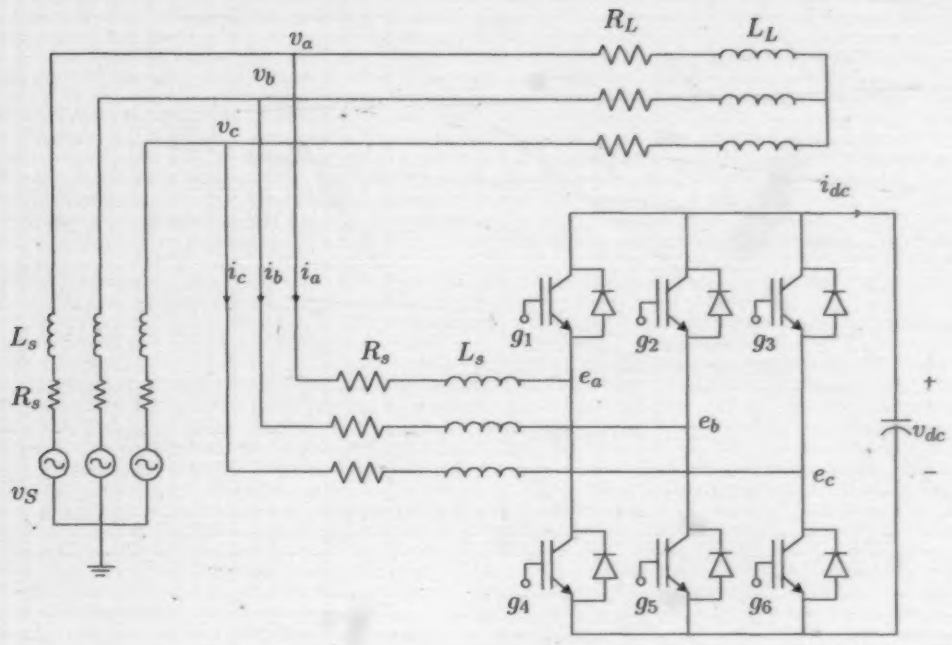


Figure 1.6: STATCOM

how power factor correction is performed. Due to the inductive load X_L, the current I_L lags the voltage source V_S by δ. I_L can be broken down into two components: the component that is in phase with V_S, i.e $I_{L,d}$ (the real component) and the component that is lagging $I_{L,d}$ by 90^o, i.e $I_{L,q}$ (the reactive component). Suppose that no compensation is done, that is, $I_q = 0$. This means that $I_S = I_L$ hence, V_S and I_S are out of phase and therefore the power factor is $\cos\delta$. For maximum efficiency, the desired power factor is $\cos(\delta) = 1$. Now suppose that compensation is available and I_q can be controlled to a desired value. In this case, we can set $I_q = I_{L,q}$. This means the compensator is supplying all the reactive power demand. Hence, $I_S = I_{L,d}$ which implies that V_S and I_S are now in phase and the power factor is corrected to 1. We remark that in Figure 1.7, a controllable current source $\mathbf{I_q}$ is connected in shunt with the line and hence this type of compensation is called *shunt compensation.*

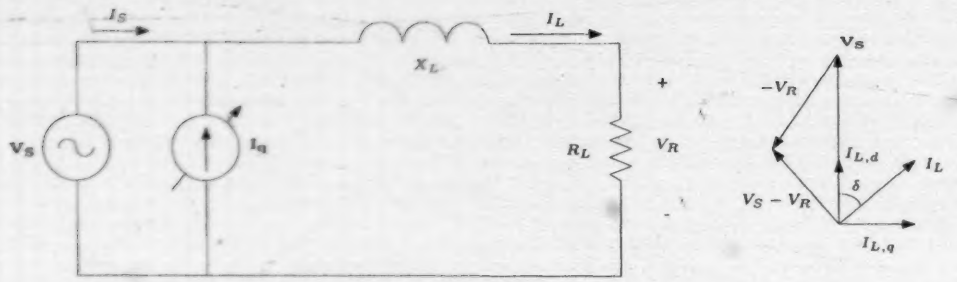


Figure 1.7: Power factor correction by STATCOM

1.2 Literature Review

Initial work on the control of the reactive power and the DC voltage of VSCs is in [26] where decoupled d-q vector control was implemented using a linearized model and PI compensators. This work established a commonly used cascade controller structure where AC currents are controlled by two decoupled PI control loops. DC voltage is controlled in a PI outer loop feeding a d-axis (real) current inner loop. This approach has enjoyed considerable success [4]. For example, in [25] vector control is applied to a benchmark STATCOM system. Different control objectives are presented including power factor correction, AC voltage regulation, and DC voltage/reactive current regulation.

As the averaged model of a VSC is nonlinear, this has led to the application of nonlinear control methods which compensate for system nonlinearity without performing a linear approximation step. By avoiding this approximation, nonlinear control offers the potential for higher performance over a wide range of operating conditions. Original work on nonlinear control is in [24] where input-output linearization is applied with the tracking output taken as a linear function of state. More recently a number of authors have reconsidered input-output linearization with a simple tracking output: the d-axis current and DC voltage, e.g. [15, 17]. The last work also shows that choosing the output as the d and q-axis currents leads to zero-dynamics which are asymptotically stable. The first application of differential flatness to the VSC is in [9, 10]. This work demonstrates the non-obvious fact that choosing the DC voltage

and the stored system energy as the linearizing or flat outputs, we can fully linearize the system without zero dynamics. This work suffers from two drawbacks; it does not derive the flat output and does not experimentally validate the nonlinear control. This thesis addresses these two issues and compares the flatness-based control with a traditional PI cascade as in [26]. This thesis also illustrates the well-known benefit of flatness for achieving motion planning in order to steer the system between two operating points while respecting input constraints. As well, unlike in [9, 10], which considers the control of DC voltage and d-axis current typical for motor drive applications, we focus on the D-STATCOM application where no load is present on the DC side (floating DC capacitor), and the objective is to track DC voltage and reactive power (i.e., q-axis current).

1.3 Thesis Contribution

In this thesis we investigate the development and the experimental validation of a novel flatness-based control technique for a Pulse Width Modulated (PWM) VSC system for STATCOM application where the DC voltage regulation and reactive power control is the main objective. The main contributions of this thesis are as follows.

- A nonlinear control for the averaged VSC model is derived using feedback linearization. No previous work has provided the derivation of this control.
- The fact that the system is locally static state feedback linearizable implies that it is also differentially flat. Flat outputs allow for offline trajectory planning in order to meet a number of control objectives and satisfy system constraints. A numerical optimization method is used to solve the motion planning problem.
- An experimental setup is developed at the Real-Time eXperimental LABoratory (RTX-LAB) at the University of Alberta. This setup validates

the proposed flatness-based nonlinear state feedback control. A sinusoidal PWM (sine PWM) is implemented on an FPGA hardware. The proposed control is compared with the conventional vector control method.

1.4 Thesis Outline

The presentation of this thesis is organized as follows:

- Chapter 2 gives a basic overview of the VSC in terms of its function and operation as well as background knowledge in power systems including PWM and reference frame theory.
- Chapter 3 focuses on the modeling of the 3-phase PWM VSC system in the original and synchronously rotating reference frames.
- Chapter 4 discusses nonlinear control including the notions of feedback linearization and flatness-based control.
- In Chapter 5, the proposed nonlinear control technique is tested on the experimental setup. This chapter provides a detailed description of the setup, the PWM implementation on the FPGA, and the control implementation using the real-time simulator. An experimental comparison with the traditional vector control system is given.
- A summary of the results, conclusions, and future work is given in Chapter 6.

Chapter 2

Background

This chapter presents a detailed description of the VSC system including its functionality and different operating modes. In addition, it is necessary to review some important principles in power systems that will be used in later chapters such as sine PWM and Reference Frame Theory.

2.1 Overview of the Voltage Source Converter

2.1.1 6-pulse VSC Configuration

A basic 6-pulse VSC consists of 6 controllable switches and 6 diodes. It is a combination of a rectifier and an inverter which allows bi-directional power flow between an AC and a DC terminal. Each controllable switch can be turned on and off by applying a digital signal called the gating signal to the gate terminal of the device. Several commonly used controllable switches include bipolar junction transistors (BJTs), gate turn off (GTO) thyristors, insulated gate bipolar transistors (IGBTs), and newly developed integrated gate commutated thyristors (IGCTs). GTOs are generally used for high power applications whereas IGBTs are used in medium power applications. The Insulated Gate Bipolar Transistors (IGBTs) are becoming a popular choice for power switching devices due to their high performance including high switching speed, low conduction loss, high current carrying capability and robustness.

The switches are digitally controlled such that when the gate terminal voltage of the device is high, the switch turns on and when the gate terminal voltage is low, the switch turns off. The gating signals for the switches are

generated by a sinusoidal Pulse Width Modulation (sine PWM) scheme so that, with proper filtering of switching harmonics, sinusoidally varying voltages appear at the AC terminals of the VSC. In order to implement sine PWM, a modulation index and a phase angle of the PWM control signal must be specified. Therefore, from a controls perspective, these two variables are the control inputs to the plant which is composed of an AC voltage supply, filter inductors, a DC capacitor, a VSC, and a PWM pulse generator. The outputs of the plant can vary depending on the operating mode, but for the STATCOM application the AC currents and the DC voltage measurements of the VSC can be considered to be the outputs (3 outputs: 2 currents and 1 voltage). Hence, the control objective is to adjust the modulation index and the phase angle of the sine PWM such that the currents and/or the voltage of the VSC can be controlled.

Figure 2.1 shows the actual VSC that is used for the experimental setup and Figure 2.2 is the equivalent circuit diagram of the VSC which consists of 6 IGBTs and 6 anti-parallel diodes. An IGBT only allows current flow in one direction, i.e., the direction of the arrow shown in the diagram, therefore in order to allow bi-directional current flow, an anti-parallel diode must be connected. A capacitor is also added on the DC terminal to maintain a constant DC voltage. Values e_a, e_b, and e_c represent the 3-phase voltages at the AC terminals and $g_1, \cdots, g_6$ are the binary gating signals where a 0 represents the open state of the switch and a 1 represents the closed state.

2.1.2 Modes of Operation

The VSC can be operated in a number of modes [25].

Reactive current control mode

Reactive current control is used mainly for power factor correction purposes, where the VSC supplies or absorbs the reactive power demand of the load. This results in reactive current control of the VSC.

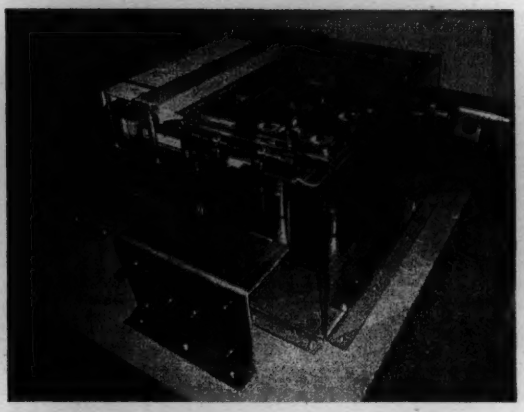


Figure 2.1: Real VSC system

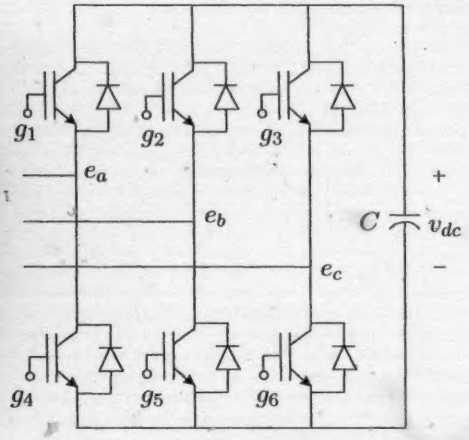


Figure 2.2: Circuit diagram of VSC

AC voltage regulation mode

AC line voltages can be regulated by supplying the appropriate amount of reactive current into the line. This can be illustrated using Figure 1.6 from Chapter 1, where the voltages v_a, v_b, and v_c can be influenced by controlling the reactive current. Suppose that the reactive current flow into the load is $I_{L,q}$ and the reactive current flow in the VSC is I_q, then if we denote the rms value of v_{abc} to be v_{rms}, we have

$$v_s - v_{rms} = I_{L,q}L_s + I_qL_s.$$

Therefore we can set the desired value for v_{rms} which will give the reference value for I_q and then the reactive current controller can be applied. Using this approach, a STATCOM can also be used for voltage flicker compensation.

DC voltage regulation mode

The DC voltage is controlled by regulating the amount of current entering into the capacitor bank. The converter draws a real power and stores it into the capacitor, therefore, by controlling the real current flow (the current component that is in phase with the voltage) of the AC side of the converter, the DC voltage can be regulated. We remark that power factor correction and AC voltage regulation cannot both be achieved simultaneously. However, it is possible to achieve both power factor correction and DC voltage regulation.

Figure 2.3: Experimental setup

2.1.3 Experimental Setup

In this thesis, we are particularly interested in controlling the reactive current and the DC voltage of the VSC. The experimental setup shown in Figure 2.3 resembles the STATCOM system where the 3-phase AC supply is connected to the AC side of the VSC via the filter inductors and the DC capacitor is floating. The voltages are measured using differential probes and the currents are measured using current sensors mounted on the VSC. These measurements are sent back to the digital simulator (controller) through the patch panel. A thorough description of the experimental setup is given in Chapter 5.

2.2 Sinusoidal Pulse Width Modulation

In this section we discuss the single-phase sine PWM in detail to illustrate how the gating signals are generated [23]. Although the actual system is a 3-phase converter, studying the single-phase PWM simplifies the discussion. In Chapter 3 we extend this work to 3-phase sine PWM.

The sine PWM pulse generator compares the modulating signal with a high frequency triangular carrier wave and outputs a high digital signal if the control wave is greater than the carrier wave and outputs a low digital signal

otherwise. The sinusoidal modulating signal is defined by

$$v_{mod} = m_a \sin(\omega t + \delta) \tag{2.1}$$

where m_a is the modulation index and δ is the phase shift. It is important to note that

$$0 \leq m_a \leq 1, \quad -\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2}.$$

If m_a becomes greater than 1 the sine PWM results in a slightly different modulating technique. This is known as *over-modulation*. For modeling purposes we want to ensure that m_a does not exceed 1. The amplitude of the carrier wave is defined to be 1. We remark that By defining v_{mod} this way, the duty ratio varies sinusoidally thereby producing a sinusoidal fundamental voltage component at the AC terminals.

Figure 2.4 (a) shows the PWM pulse generation scheme for a single-phase system where the two signals are being compared to generate the gating pulses in (b). Since Digital Signal Processors (DSPs) or other digital devices (e.g. FPGAs) are generally used for PWM generation, v_{mod} in reality is not an ideal smooth sine wave but rather a discrete waveform $v_{mod,d}$ as shown in Figure 2.4 (c) and (d). Note that in Figure 2.4 (c) the time step of $v_{mod,d}$ is half the period of the carrier wave v_c. It is also possible to have the time step of the modulating signal equal to the period of v_c as in Figure 2.4 (d). The typical frequency of the carrier wave f_c is $1-4$ kHz. The sinusoidal modulation signal has the frequency of around $50-60$ Hz.

For simplicity, a single-phase one-leg inverter is shown in Figure 2.5. Here we assume that v_{dc} is constant. The two pulses generated by the sine PWM are sent to the upper and the lower switches of the bridge. Note that g_1 and g_2 are compliments of each other so that the pulses will not create a short circuit. For hardware implementation, a *dead-time* or *blanking time* must be inserted to ensure that both switches are not closed at any given time to avoid short-circuiting and potentially damaging the system [23]. Figure 2.6 shows the dead-time implementation. Signals g_1, g_2 are the digital pulses generated by the sine PWM before dead-time is added and g_1', g_2' are the pulses after dead-time is added. We note that only the rising edges of each signal is delayed

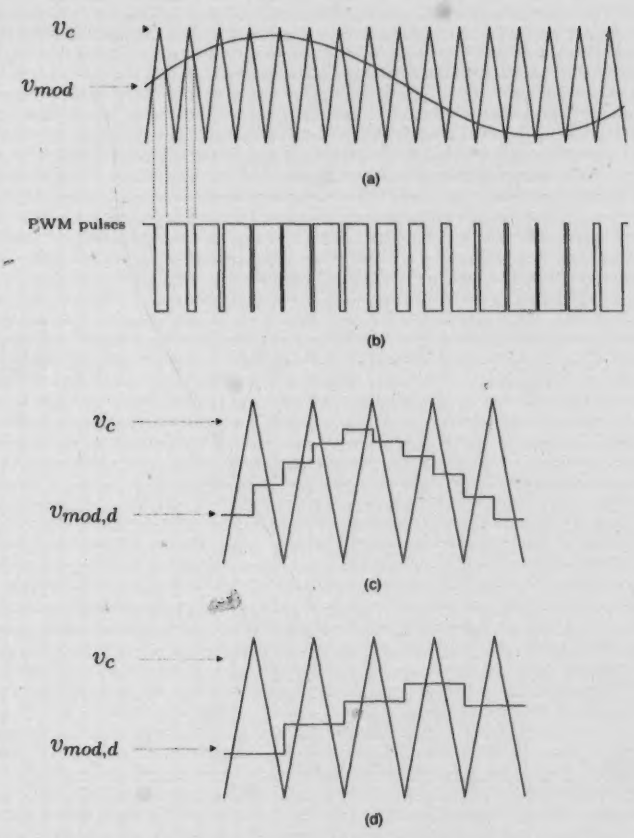


Figure 2.4: Sine PWM pulse generation

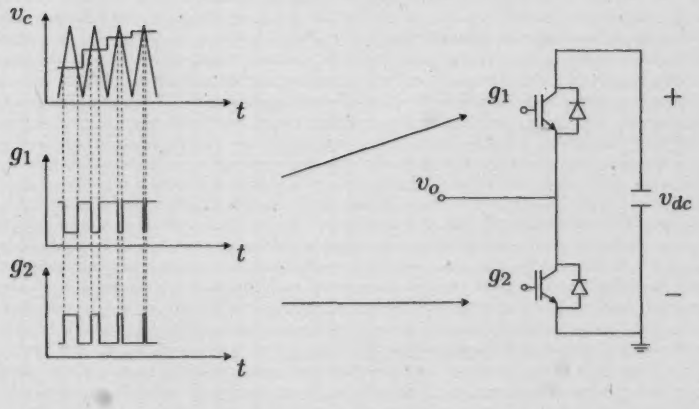


Figure 2.5: Sine PWM pulses for the single bridge system

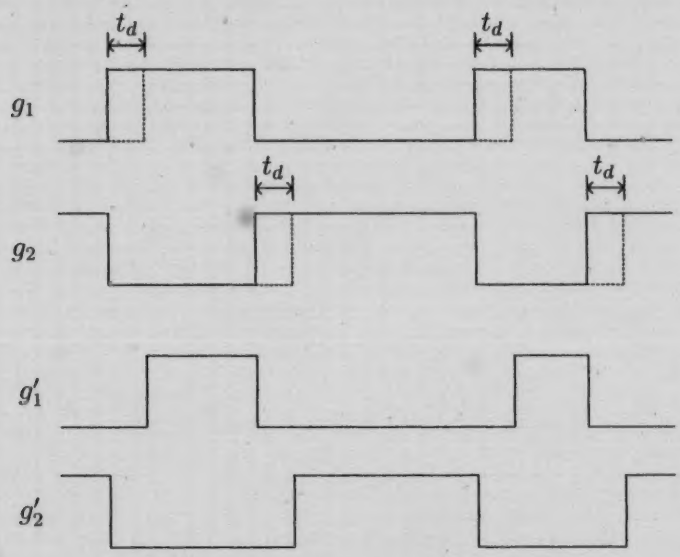


Figure 2.6: Dead-time implementation

by a small time t_d. By doing this, the danger of both switches simultaneously closing can be avoided.

From Figure 2.5, when $g_1 = 1$, $g_2 = 0$, the output voltage v_o equals v_{dc}, and when $g_1 = 0$, $g_2 = 1$, v_o equals 0. Note that in this circuit the ground is the negative side of the capacitor. Hence, as shown in Figure 2.8, v_o is a fast switching square wave. A typical approach in modeling this waveform is to take the fundamental component of this voltage, or equivalently, taking the average of v_o over each period of the carrier wave v_c. To illustrate this consider Figure 2.7. The averaged voltage $v_{o,avg}$ is obtained by the following.

$$\begin{aligned} v_{o,avg} &= \frac{v_{mod}}{2\hat{v}_c} \cdot v_{dc} + \left(1 - \frac{v_{mod}}{2\hat{v}_c}\right) \cdot 0 \\ &= v_{mod}\frac{v_{dc}}{2} \end{aligned}$$

where the peak voltage of the carrier wave $\hat{v}_c$ is 1. Now we let v_{mod} have a modulation index of m_a and have a frequency of ω rad/s with a phase shift of δ. Assuming that the carrier frequency is sufficiently higher than the frequency

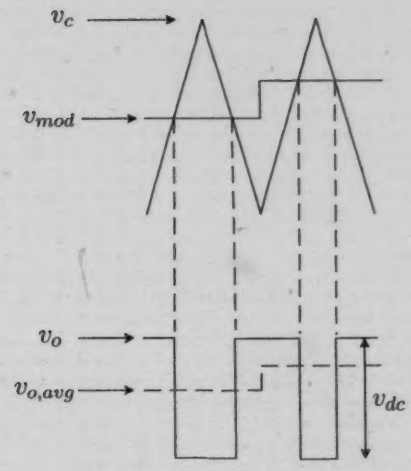


Figure 2.7: Averaging of v_o

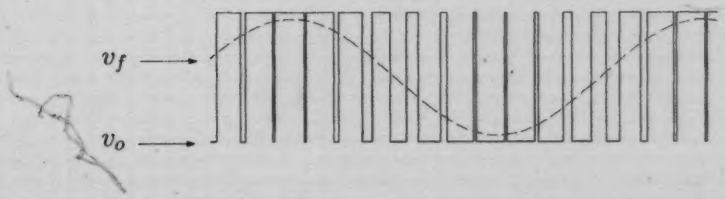


Figure 2.8: Output voltage v_o and its fundamental component v_f

of v_{mod} and that v_{mod} can be approximated to be a smooth sine wave, we have

$$\begin{aligned} v_{mod} &\approx m_a \sin(\omega t + \delta) \\ v_{o,avg} &\approx m_a \sin(\omega t + \delta)\frac{v_{dc}}{2} \\ &= \frac{1}{2} m_a v_{dc} \sin(\omega t + \delta) \end{aligned} \tag{2.2}$$

We remark that the average value $v_{o,avg}$ is the same as the fundamental frequency component of v_o which is shown as a dashed line in Figure 2.8. Hence, we have shown that in a single-bridge inverter system the averaged AC terminal voltage is (2.2). In the next chapter we show that this equation is also valid for the 3-phase system with 3 bridges.

2.3 Reference Frame Theory

In 3-phase power electronic devices or machines, it is often the case that some variables such as AC voltages and currents are sinusoidally varying under normal operations and this creates complexity in modelling. The purpose of the Reference Frame Transformation (RFT) is to apply a change of variables to these signals so that, in the new reference frame, the model equations are simplified. In a 6-pulse VSC, it is desirable to apply this transformation so that all the AC signals of the system become constant under steady state operation. This can be achieved by performing a *Synchronously Rotating* Reference Frame Transformation. There are several different types of reference frame transformations but they can all be summarized into one general form. The Synchronously Rotating RFT is one specific form of this general transformation. Detailed information on reference frame theory can be found in [14].

2.3.1 General Reference Frame Transformation

A transformation of the 3-phase variables f_{abc} from an original reference frame (abc components) to an arbitrary reference frame (dqo components) can be expressed as

$$f_{dqo} = K f_{abc}$$

where

$$f_{abc} = \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}, \quad f_{dqo} = \begin{bmatrix} f_d \\ f_q \\ f_o \end{bmatrix}$$

$$K = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.3}$$

$$\omega = \frac{d\theta}{dt}.$$

It can be shown that the inverse transformation of K is

$$K^{-1} = \frac{3}{2} K^T = \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{\sqrt{2}} \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix}.$$

Here, the angular velocity ω and the angular displacement θ are unspecified, therefore this is the most general form of the RFT. We remark the non-uniqueness of the transformation matrix K. It is also possible to have

$$K = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

which gives the same transformation. The important thing is that the d-component is leading the q-component by 90°. Figure 2.9 shows the three

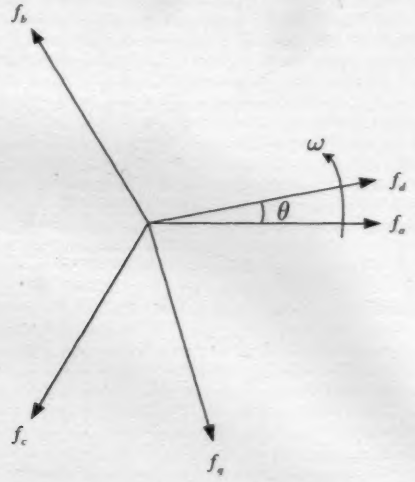


Figure 2.9: Arbitrary reference frame transformation

stationary components f_a, f_b, f_c that are 120° apart from each other, and the d-q component f_d, f_q after the transformation which is rotating at an angular velocity of ω. The angle between f_a and f_d is θ and f_q is 90 degrees out of phase from f_d, where the subscript d and q represents *direct* and *quadrature*, respectively.

2.3.2 Synchronously Rotating Reference Frame

Now we assume that f_a, f_b, f_c are a 3-phase balanced set that is rotating at an angular velocity of ω_e. Hence,

$$f^e_{abc} = \begin{bmatrix} f^e_a \\ f^e_b \\ f^e_c \end{bmatrix} = \begin{bmatrix} \hat{f}_a \cos(\omega_e t) \\ \hat{f}_b \cos(\omega_e t - \frac{2\pi}{3}) \\ \hat{f}_c \cos(\omega_e t + \frac{2\pi}{3}) \end{bmatrix}.$$

Then

$$f^e_{dqo} = K^e f^e_{abc}$$

where

$$f^e_{abc} = \begin{bmatrix} f^e_a \\ f^e_b \\ f^e_c \end{bmatrix}, \quad f^e_{dqo} = \begin{bmatrix} f^e_d \\ f^e_q \\ f^e_o \end{bmatrix}$$

$$K^e = \frac{2}{3} \begin{bmatrix} \cos(\omega_e t) & \cos(\omega_e t - \frac{2\pi}{3}) & \cos(\omega_e t + \frac{2\pi}{3}) \\ -\sin(\omega_e t) & -\sin(\omega_e t - \frac{2\pi}{3}) & -\sin(\omega_e t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}.$$

Therefore, from (2.3), we have made the following substitution.

$$\theta = \omega_e t.$$

In this case, f_d, f_q are rotating at an angular velocity of ω_e which is the same speed at which the original variables f^e_{abc} are rotating.

2.4 Summary

In this chapter, we described the 6-pulse VSC system, its modes of operation and control objectives. Sine PWM and reference frame transformation were explained. In the next chapter, we use this background knowledge to derive our model for the VSC.

Chapter 3

Averaged Modeling of the PWM 6-pulse VSC

In this chapter, a dynamic behavior of the 6-pulse VSC is mathematically modeled. Since the PWM introduces high frequency switching harmonics to the system, the exact mathematical modeling of the AC terminal voltages of the VSC is difficult [18]. Therefore, an approximate averaged model is derived which ignores the high frequency harmonics. The averaged modeling of the VSC leads to 4 dynamic equations: 3 equations for the AC side of the VSC, and 1 equation for the DC side. In an actual system, the 3-phase AC voltages are assumed balanced, and this suggests that having 3 dynamic equations for the AC terminal dynamics is redundant and can be reduced to 2 equations. This can be achieved by a synchronously rotating reference frame transformation known as *d-q transformation* where the d-axis of the d-q frame is in phase with the a-axis of the original frame. In addition, in d-q frame the AC components are constants under steady state operation.

3.1 Mathematical Model Derivation

Figure 3.1 shows the 6-pulse VSC that is used for modeling the dynamics of the system. The phase voltages v_a, v_b, v_c are the 3-phase balanced AC voltage source, the phase currents are denoted i_a, i_b, i_c, and the AC terminal voltages of the VSC are denoted e_a, e_b, e_c. The gating signals $g_1, \cdots, g_6$ are binary values of the switches where 1 represents a closed configuration of the switch and 0

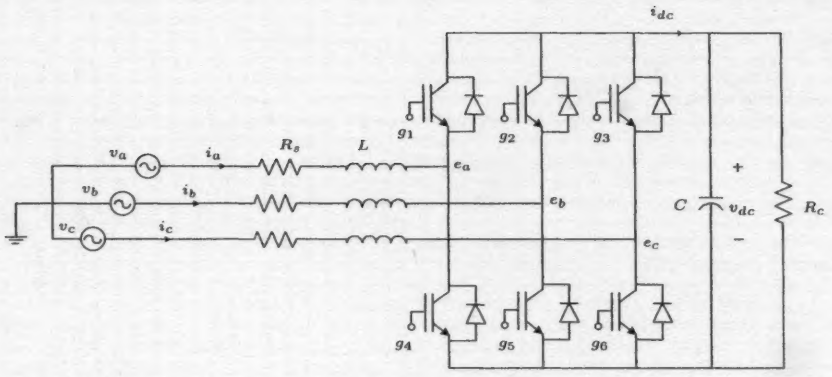


Figure 3.1: Circuit diagram of the VSC model

represents an open switch. We note that g_i and g_{i+3} are compliments of each other for $i = 1, 2, 3$. The line losses and the transformer conduction losses are modelled by R_s, and the inverter switching losses are modelled by the shunt resistance R_c [26]. Hence, the switches and diodes are assumed lossless. Filter inductors L are connected between the AC side of the converter and the AC supply in order to filter out switching harmonics of the voltages introduced by the PWM. Although it is possible to achieve negative DC voltage, most STATCOM applications require $v_{dc} > 0$. The 3-phase balanced AC source is modeled as

$$\begin{aligned} v_a &= \hat{V} \sin(\omega t) \\ v_b &= \hat{V} \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_c &= \hat{V} \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned}$$

where ω is an angular frequency of the AC source. Using Kirchoff's voltage and current law, the following equations can be obtained from the circuit diagram.

$$\begin{aligned} L\frac{di_a}{dt} + R_s i_a &= v_a - e_a \\ L\frac{di_b}{dt} + R_s i_b &= v_b - e_b \\ L\frac{di_c}{dt} + R_s i_c &= v_c - e_c \end{aligned}$$

or simply

$$L\frac{d}{dt}i_{abc} + R_s i_{abc} = v_{abc} - e_{abc}$$

where

$$v_{abc} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad i_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad e_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

Since the switches and diodes of the VSC are assumed ideal, the instantaneous power at the AC terminals of the VSC is equal to that of the DC terminal, giving the following power balance equation:

$$i_a e_a + i_b e_b + i_c e_c = i_{dc} v_{dc}$$

which leads to

$$i_{dc} = C\frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_c} = \frac{i_a e_a + i_b e_b + i_c e_c}{v_{dc}}$$

or

$$\frac{dv_{dc}}{dt} = \frac{i_a e_a + i_b e_b + i_c e_c}{C v_{dc}} - \frac{v_{dc}}{C R_c}$$

The actual system in the experimental setup has the parameters given in Table 3.1. The 3-phase AC source supplies a line-to-line voltage of 100 V_{rms} which implies $v_d = \hat{V} = 81.65$ V.

Parameter	Value
R_s	0.23 Ω
C	0.0033 F
R_c	18000 Ω
v_d	81.65 V
L	0.0025 H
ω	120π rad/s

Table 3.1: Model parameters

3.1.1 3-phase Sine PWM

Since the sine PWM pulses are controlling the switches at high frequency, it can be expected that the voltages e_{abc} contain high frequency switching harmonics. We want to model the fundamental component or the averaged values of these voltages in terms of the modulation index m_a, phase shift δ,

and the DC voltage. Although there are 6 switches to be controlled, since two switches in the same bridge are compliments of each other, only 3 control signals for the 3-phase sine PWM are required. Therefore, we have

$$v_{mod,a} = m_a \sin(\omega t + \delta)$$
$$v_{mod,b} = m_a \sin\left(\omega t - \frac{2\pi}{3} + \delta\right)$$
$$v_{mod,c} = m_a \sin\left(\omega t + \frac{2\pi}{3} + \delta\right)$$

where subscript *mod* stands for *modulation*. Note that the carrier wave v_c is the same for all 3 phases. Now the 6 gating pulses are generated according to the following law:

$$(g_1, g_4) = \begin{cases} (1,0) & \text{if } v_{mod,a} \geq v_c \\ (0,1) & \text{otherwise} \end{cases}$$
$$(g_2, g_5) = \begin{cases} (1,0) & \text{if } v_{mod,b} \geq v_c \\ (0,1) & \text{otherwise} \end{cases}$$
$$(g_3, g_6) = \begin{cases} (1,0) & \text{if } v_{mod,c} \geq v_c \\ (0,1) & \text{otherwise.} \end{cases}$$

Figure 3.2 shows the waveforms for the 3-phase sine PWM.

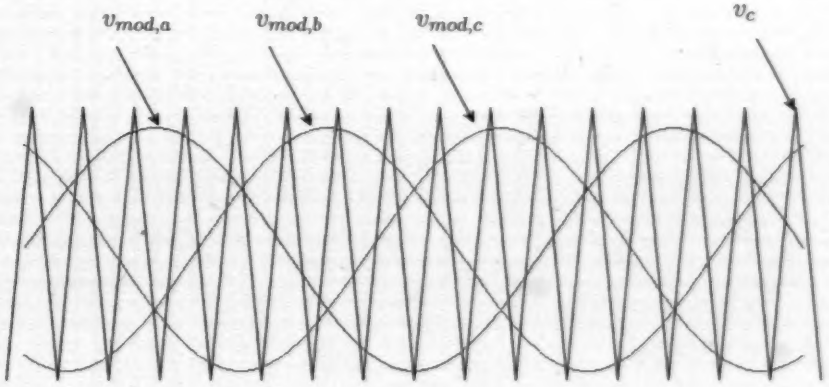


Figure 3.2: 3-phase sine PWM

3.1.2 Averaged Modeling of the AC Terminals

The instantaneous voltages at the AC terminals can be found by considering each switch configuration. Only considering the top three switches g_1, g_2, and

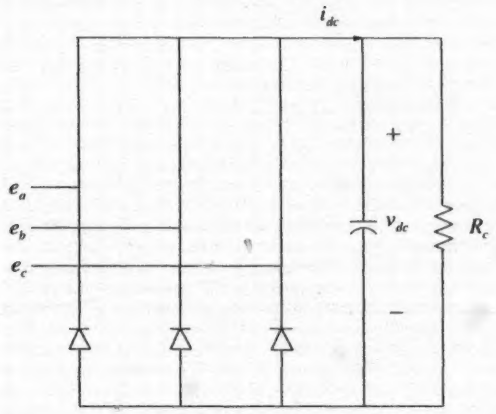


Figure 3.3: Circuit diagram of the VSC when $g_1 = g_2 = g_3 = 1$

g_3, there are 8 possible switch configurations ($2^3 = 8$). We look at some of these configurations in detail to see how the voltages are affected by the switches. Analyzing all 8 possible configurations is unnecessary and we consider the 3 unique cases.

case 1. $g_1 = 1$, $g_2 = 1$, $g_3 = 1$. Since all the top switches are closed (and hence the bottom three switches are open), e_a, e_b, and e_c are shorted, i.e.,

$$e_a = e_b = e_c$$

And also an assumption that the 3 phase AC source is balanced gives

$$e_a + e_b + e_c = 0$$

and therefore,

$$e_a = e_b = e_c = 0$$

Figure 3.3 shows the diagram of the VSC for this switch configuration.

case 2. $g_1 = 1$, $g_2 = 1$, $g_3 = 0$. See Figure 3.4. In this case

$$e_a = e_b$$

$$e_a - e_c = v_{dc}$$

$$e_a + e_b + e_c = 0$$

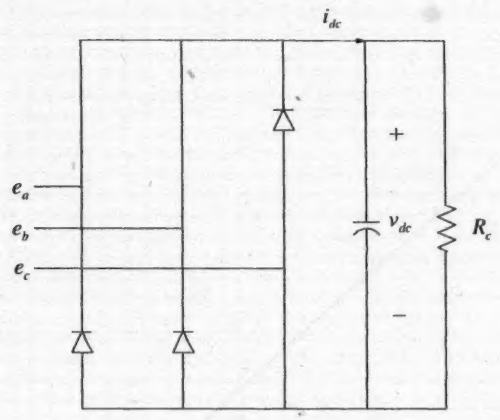


Figure 3.4: Circuit diagram of the VSC when $g_1 = g_2 = 1, g_3 = 0$

which leads to,

$$e_a = \frac{1}{3}v_{dc}, \quad e_b = \frac{1}{3}v_{dc}, \quad e_c = -\frac{2}{3}v_{dc}$$

case 3. $s_a = 1$, $s_b = 0$, $s_c = 0$. See Figure 3.5. Similarly,

$$e_b = e_c$$
$$e_a - e_b = v_{dc}$$
$$e_a + e_b + e_c = 0$$

which gives,

$$e_a = \frac{2}{3}v_{dc}, \quad e_b = -\frac{1}{3}v_{dc}, \quad e_c = -\frac{1}{3}v_{dc}$$

The same approach can be taken for the remaining switch configurations and we obtain Table 3.2. Therefore, we conclude that, at any instant, the VSC takes on one of these 8 possible switch configurations. We also note that the possible voltages that e_a, e_b, and e_c can take at any instant are in the set

$$\left\{0, \pm\frac{v_{dc}}{3}, \pm\frac{2v_{dc}}{3}\right\}$$

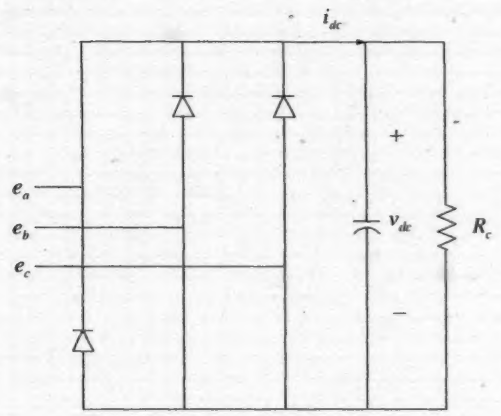


Figure 3.5: Circuit diagram of the VSC when $g_1 = 1, g_2 = g_3 = 0$

In the next section, we discuss how the VSC switches between these configurations when driven by a sine PWM scheme.

As mentioned earlier, if the control sampling frequency f_s and the carrier wave frequency f_c are the same, then the control modulating signal v_{mod} is piecewise constant over each period of the carrier wave. On the other hand, if $f_s = 2f_c$ then the v_{mod} is constant over a half of the carrier wave period. Since both cases result in the same analysis, we will assume that $f_s = f_c$ for simplicity although in the real experimental setup $f_s = 2f_c$. In the case of a 3-phase system, we have 3 control modulating signals which are all being compared to a single carrier wave. In Figure 3.6 the diagram is partitioned into 6 regions where in each region the three control signals do not crossover. For example, in Region 1

$$v_{mod,a} \geq v_{mod,b} \geq v_{mod,c}$$

and the indices a, b, c indicate this relationship. Next we look at each region to see how the voltage e_a is affected by the three phase modulating signals.

Region 1. In this region $v_{mod,a} \geq v_{mod,b} \geq v_{mod,c}$ and this leads to Figure 3.7. For simplicity, the figure only shows voltage e_a. The numbers below indicate the switching configuration of (g_1, g_2, g_3) for each step, and referring to Table 3.2, the value for e_a can be found. Therefore, in Region 1, e_a

(g_1, g_2, g_3)	e_a	e_b	e_c
(1,1,1)	0	0	0
(1,1,0)	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$	$-\frac{2}{3}v_{dc}$
(1,0,1)	$\frac{1}{3}v_{dc}$	$-\frac{2}{3}v_{dc}$	$\frac{1}{3}v_{dc}$
(1,0,0)	$\frac{2}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$
(0,1,1)	$-\frac{2}{3}v_{dc}$	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$
(0,1,0)	$-\frac{1}{3}v_{dc}$	$\frac{2}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$
(0,0,1)	$-\frac{1}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$	$\frac{2}{3}v_{dc}$
(0,0,0)	0	0	0

Table 3.2: The voltages e_{abc} for each switch configuration

is a staircase shaped voltage where each step has a height of $\frac{1}{3}v_{dc}$. It is difficult to represent this voltage in a mathematical equation but we can obtain an approximate relation by taking the average value of e_a over each period of the triangular wave. We remark that the average of e_a over one period and the average of e_a over a half of the period are the same due to symmetry. The average value of e_a over one period of carrier wave is

$$\begin{aligned} e_{a,ave} &= \frac{v_{mod,c}+1}{2}\cdot 0 + \frac{v_{mod,b}-v_{mod,c}}{2}\cdot\frac{v_{dc}}{3} + \frac{v_{mod,a}-v_{mod,b}}{2}\cdot\frac{2v_{dc}}{3} \\ &= \frac{v_{dc}}{6}(2v_{mod,a}-v_{mod,b}-v_{mod,c}) \end{aligned}$$

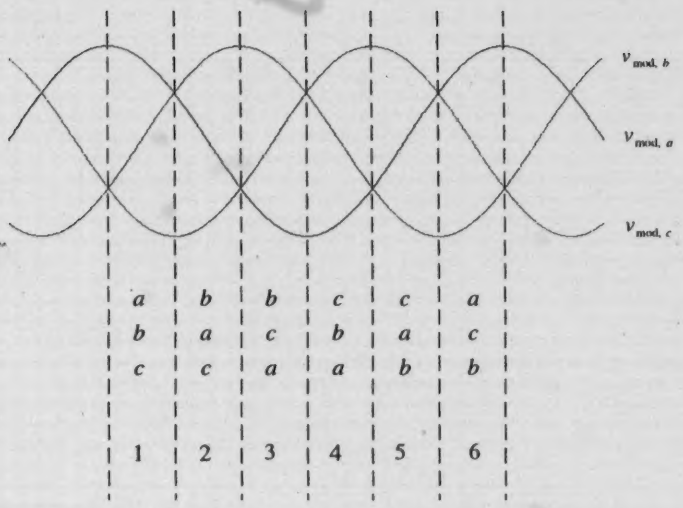


Figure 3.6: 3-phase control signals with 6 regions

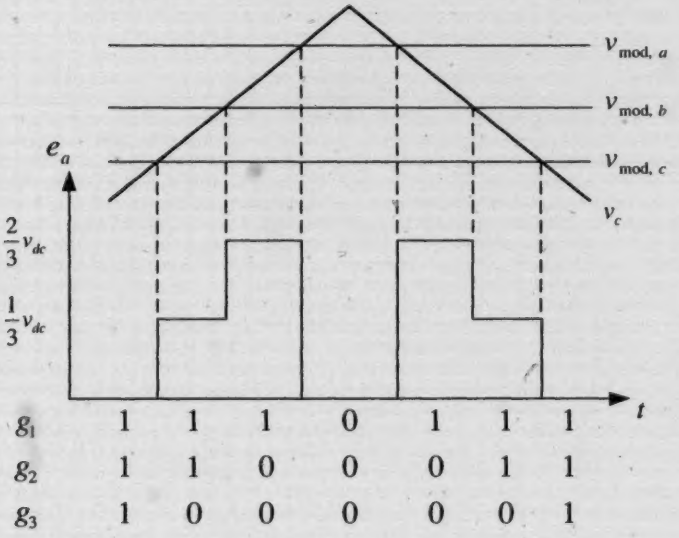
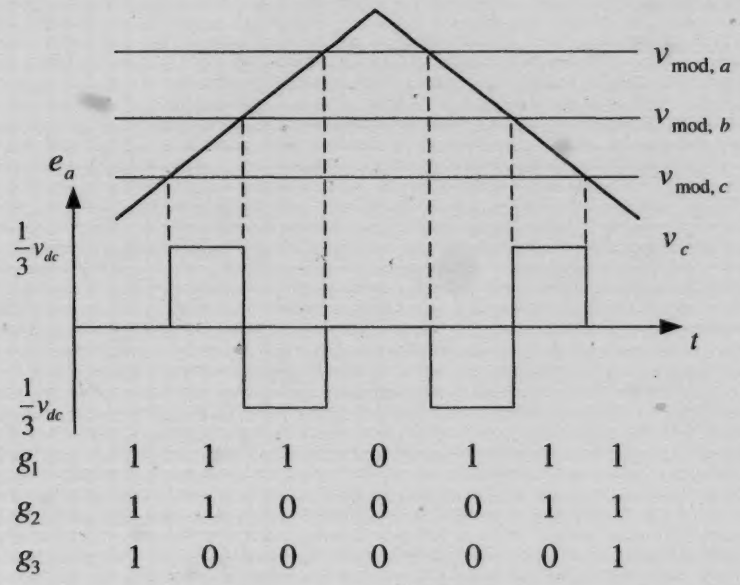


Figure 3.7: The value of e_a when $v_{mod,a} \geq v_{mod,b} \geq v_{mod,c}$

Region 2. Figure 3.8 shows the pulses of e_a when $v_{mod,b} \geq v_{mod,a} \geq v_{mod,c}$. By taking the similar approach as in Region 1, we obtain the waveform of e_a shown in the figure. The average voltage of e_a in this case is



g_1	1	1	1	0	1	1	1
g_2	1	1	0	0	0	1	1
g_3	1	0	0	0	0	0	1

Figure 3.8: The value of e_a when $v_{mod,b} \geq v_{mod,a} \geq v_{mod,c}$

$$e_{a,avg} = \frac{v_{mod,c}+1}{2} \cdot 0 + \frac{v_{mod,a}-v_{mod,c}}{2} \cdot \frac{v_{dc}}{3} + \frac{v_{mod,b}-v_{mod,a}}{2} \cdot -\frac{v_{dc}}{3}$$
$$= \frac{v_{dc}}{6}(2v_{mod,a} - v_{mod,b} - v_{mod,c})$$

Region 3. In this region $v_{mod,b} \geq v_{mod,c} \geq v_{mod,a}$ and therefore we obtain the waveforms shown in Figure 3.9. The average value of e_a over one cycle of carrier wave is

$$e_{a,avg} = \frac{v_{mod,a}+1}{2} \cdot 0 + \frac{v_{mod,c}-v_{mod,a}}{2} \cdot -\frac{2v_{dc}}{3} + \frac{v_{mod,b}-v_{mod,c}}{2} \cdot -\frac{v_{dc}}{3}$$
$$= \frac{v_{dc}}{6}(2v_{mod,a} - v_{mod,b} - v_{mod,c})$$

So far, we have analyzed the AC terminal voltage e_a for the first three regions of Figure 3.6. Although the figure shows 6 separate regions, it turns out that Regions 1 and 6, 2 and 5, and 3 and 4 have the identical waveforms for e_a, e_b, e_c. We also conclude that regardless of the region, the average value of e_a over one period of the carrier wave is

$$e_{a,avg} = \frac{v_{dc}}{6}(2v_{mod,a} - v_{mod,b} - v_{mod,c}) \tag{3.1}$$

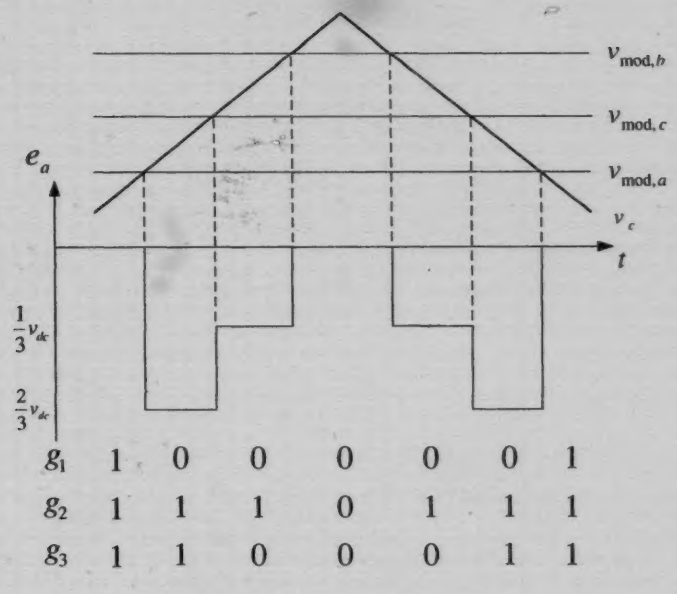


Figure 3.9: The value of e_a when $v_{mod,b} \geq v_{mod,c} \geq v_{mod,a}$

If we substitute

$$\begin{aligned} v_{mod,a} &= m_a \sin(\omega t + \delta) \\ v_{mod,b} &= m_a \sin\left(\omega t - \frac{2\pi}{3} + \delta\right) \\ v_{mod,c} &= m_a \sin\left(\omega t + \frac{2\pi}{3} + \delta\right) \end{aligned}$$

into (3.1) we have

$$\begin{aligned} e_{a,ave} &= \frac{v_{dc}}{6}\left(2m_a \sin(\omega t + \delta) - m_a \sin(\omega t - \frac{2\pi}{3} + \delta) - m_a \sin(\omega t + \frac{2\pi}{3} + \delta)\right) \\ &= \frac{v_{dc}}{6}\left[2m_a \sin(\omega t + \delta) - m_a\left(\sin(\omega t + \delta)\cos(\frac{2\pi}{3}) + \sin(\omega t + \delta)\cos(\frac{2\pi}{3})\right)\right] \\ &= \frac{v_{dc}}{6}\left[3m_a \sin(\omega t + \delta)\right] \\ &= \frac{1}{2}v_{dc}m_a \sin(\omega t + \delta) \end{aligned}$$

Note that this equation is identical to (2.2) for the single phase case as discussed in Chapter 2. By taking the similar approach for phases b and c, we obtain the following averaged model for the 3-phase AC terminal voltages of

the VSC:

$$
\begin{aligned}
e_{a,ave} &= \frac{1}{2} v_{dc} m_a \sin(\omega t + \delta) \\
e_{b,ave} &= \frac{1}{2} v_{dc} m_a \sin\left(\omega t - \frac{2\pi}{3} + \delta\right) \\
e_{c,ave} &= \frac{1}{2} v_{dc} m_a \sin\left(\omega t + \frac{2\pi}{3} + \delta\right).
\end{aligned} \tag{3.2}
$$

3.2 d-q Transformation

In this section, we discuss reference frame transformation from a stationary to a synchronously rotating reference frame which we call *d-q transformation* which enables the sinusoidal currents and voltages to be separated into real and reactive components, i.e., d and q components. From the previous section we have

$$
L\frac{d}{dt} i_{abc} + R_s i_{abc} = v_{abc} - e_{abc} \tag{3.3}
$$

where

$$
v_{abc} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad i_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad e_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}.
$$

Now we apply the reference frame theory discussed in the previous chapter to represent (3.3) in d-q frame. Recall from Chapter 2 that the synchronously rotating RFT matrix K^e from an abc to a d-q frame, and its inverse $(K^e)^{-1}$ are

$$
K^e = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}
$$

$$
(K^e)^{-1} = \begin{bmatrix} \sin\omega t & \cos\omega t & \frac{1}{\sqrt{2}} \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix}.
$$

Then the dqo components of the variables are given by

$$
\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = (K^e)^{-1} \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}, \quad \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = (K^e)^{-1} \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix}, \quad \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = (K^e)^{-1} \begin{bmatrix} e_d \\ e_q \\ e_o \end{bmatrix}.
$$

The derivative of i_{abc} in d-q frame is

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{d}{dt}(K^e)^{-1}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + (K^e)^{-1}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}$$
$$= (K^e)^{-1}\begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + (K^e)^{-1}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}.$$

Substituting these into (3.3) gives

$$L(K^e)^{-1}\begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + L(K^e)^{-1}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + R_s(K^e)^{-1}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}$$
$$= (K^e)^{-1}\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} - (K^e)^{-1}\begin{bmatrix} e_d \\ e_q \\ e_o \end{bmatrix}$$

and therefore

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L} & \omega & 0 \\ -\omega & -\frac{R_s}{L} & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_d - e_d \\ v_q - e_q \\ v_o - e_o \end{bmatrix}.$$

Since we assumed the AC source to be balanced, i.e., $v_a + v_b + v_c = 0$, the third component is 0, therefore the variables with a subscript o have been omitted to give

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L} & \omega \\ -\omega & -\frac{R_s}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_d - e_d \\ v_q - e_q \end{bmatrix}. \tag{3.4}$$

Also from the power balance equation, we have

$$\frac{dv_{dc}}{dt} = \frac{i_a e_a + i_b e_b + i_c e_c}{C v_{dc}} - \frac{v_{dc}}{C R_c}. \tag{3.5}$$

Equation (3.5) can be represented in d-q frame in a following way. Since

$$\begin{aligned} e_a i_a + e_b i_b + e_c i_c &= \begin{bmatrix} e_a & e_b & e_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \\ &= e_{abc}^T i_{abc} \\ &= \left((K^e)^{-1} e_{dqo}\right)^T (K^e)^{-1} i_{dqo} \\ &= e_{dqo}^T \left((K^e)^{-1}\right)^T (K^e)^{-1} i_{dqo} \\ &= e_{dqo}^T \left(\frac{3}{2}(K^e)^T\right)^T (K^e)^{-1} i_{dqo} \\ &= e_{dqo}^T \frac{3}{2} K^e (K^e)^{-1} i_{dqo} \\ &= \frac{3}{2} e_{dqo}^T i_{dqo} \\ &= \frac{3}{2}(e_d i_d + e_q i_q + e_o i_o) = \frac{3}{2}(e_d i_d + e_q i_q) \end{aligned}$$

we have the power balance equation in d-q frame as

$$\frac{dv_{dc}}{dt} = \frac{3}{2}\frac{e_d i_d + e_q i_q}{C v_{dc}} - \frac{v_{dc}}{C R_c}. \tag{3.6}$$

Combining (3.4) and (3.6), the final expression for the VSC model in d-q frame is

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + \omega i_q + \frac{v_d}{L} - \frac{e_d}{L} \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q - \omega i_d - \frac{e_q}{L} \\ \frac{dv_{dc}}{dt} &= \frac{3}{2}\frac{e_d i_d + e_q i_q}{C v_{dc}} - \frac{v_{dc}}{C R_c}. \end{aligned} \tag{3.7}$$

We remark that the inputs to this system are the modulation index m_a and the phase shift δ of the sine PWM. The AC terminal voltages e_d and e_q can also be expressed in terms of m_a, δ, and v_{dc}. In order to derive the expressions

for e_d and e_q, we do the following calculation.

$$\begin{bmatrix} e_d \\ e_q \\ e_o \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\omega t & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

$$= \frac{2}{3}\begin{bmatrix} \sin\omega t & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} \frac{1}{2}v_{dc}m_a\sin(\omega t + \delta) \\ \frac{1}{2}v_{dc}m_a\sin(\omega t - \frac{2\pi}{3} + \delta) \\ \frac{1}{2}v_{dc}m_a\sin(\omega t + \frac{2\pi}{3} + \delta) \end{bmatrix}$$

$$= \frac{1}{3}v_{dc}m_a\cos\delta\begin{bmatrix} \sin^2\omega t + \sin^2(\omega t - \frac{2\pi}{3}) + \sin^2(\omega t + \frac{2\pi}{3}) \\ \sin\omega t\cos\omega t + \sin(\omega t - \frac{2\pi}{3})\cos(\omega t - \frac{2\pi}{3}) + \sin(\omega t + \frac{2\pi}{3})\cos(\omega t + \frac{2\pi}{3}) \\ 0 \end{bmatrix}$$
$$+ \frac{1}{3}v_{dc}m_a\sin\delta\begin{bmatrix} \sin\omega t\cos\omega t + \sin(\omega t - \frac{2\pi}{3})\cos(\omega t - \frac{2\pi}{3}) + \sin(\omega t + \frac{2\pi}{3})\cos(\omega t + \frac{2\pi}{3}) \\ \sin^2\omega t + \sin^2(\omega t - \frac{2\pi}{3}) + \sin^2(\omega t + \frac{2\pi}{3}) \\ 0 \end{bmatrix}$$

$$= \frac{1}{3}v_{dc}m_a\cos\delta\begin{bmatrix} \frac{1}{2}(\sin 2\omega t + \sin(2\omega t - \frac{4\pi}{3}) + \sin(2\omega t + \frac{4\pi}{3})) \\ \frac{3}{2} \\ 0 \end{bmatrix}$$
$$+ \frac{1}{3}v_{dc}m_a\sin\delta\begin{bmatrix} \frac{1}{2}(\sin 2\omega t + \sin(2\omega t - \frac{4\pi}{3}) + \sin(2\omega t + \frac{4\pi}{3})) \\ \frac{3}{2} \\ 0 \end{bmatrix}$$

$$= \frac{1}{3}v_{dc}m_a\cos\delta\begin{bmatrix} \frac{3}{2} \\ 0 \\ 0 \end{bmatrix} + \frac{1}{3}v_{dc}m_a\sin\delta\begin{bmatrix} 0 \\ \frac{3}{2} \\ 0 \end{bmatrix} = \frac{1}{2}v_{dc}m_a\begin{bmatrix} \cos\delta \\ \sin\delta \\ 0 \end{bmatrix}.$$

Therefore, we have

$$e_d = \frac{1}{2}v_{dc}m_a\cos\delta, \quad e_q = \frac{1}{2}v_{dc}m_a\sin\delta. \tag{3.8}$$

Substituting (3.8) into (3.7) gives

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{1}{2L}v_{dc}m_a\cos\delta \\ \frac{di_q}{dt} &= -\frac{R_s}{L}i_q - \omega i_d - \frac{1}{2L}v_{dc}m_a\sin\delta \\ \frac{dv_{dc}}{dt} &= \frac{3(i_d m_a\cos\delta + i_q m_a\sin\delta)}{4C} - \frac{v_{dc}}{CR_c} \end{aligned} \tag{3.9}$$

3.3 Summary

In this chapter we have derived the model for the 6-pulse VSC with sine PWM in d-q reference frame. The nonlinear system has 3 states (i_d, i_q, v_{dc}) and 2 inputs (m_a, δ). In fact, the system possesses a bilinear structure, i.e., the system is linear in the states but nonlinear in the control inputs [19]. The model requires that the inputs are bounded as

$$0 \leq m_a \leq 1, \quad -\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2}$$

The choice of the inputs are non-unique and this fact can be observed in previous work. For example, another choice of inputs is

$$u_1 = m_a \cos\delta$$

$$u_2 = m_a \sin\delta.$$

Chapter 4

Nonlinear Control Design of the VSC

In the previous chapter, the mathematical model for the VSC has been derived in d-q reference frame. The traditional approaches to controlling this VSC system often involves linearization of the nonlinear model about a certain operating point and a set of PI compensators are implemented in the control system [26]. In this chapter we want to develop a nonlinear model-based controller of the VSC. Since this approach will circumvent the linearization process of the model, improved performance can be expected from the nonlinear controller.

The main objective of this chapter is the development of the flatness-based trajectory tracking control. Flatness allows us to design a controller that will drive the system from one equilibrium point to another while satisfying certain control objectives or constraints. For the VSC system, the notion of flatness is closely related to the theory of feedback linearization and hence, both concepts are discussed. We also discuss the traditional vector control method which is based on a set of PI controllers in order to compare the two different control schemes.

This chapter is organized as follows: The state space model and the equilibrium set are discussed. Then feedback linearization and flatness-based control techniques are presented. The next section discusses flatness-based open loop motion planning and closed loop static state feedback control followed by simulation results. Finally, the decoupled vector control technique is discussed.

4.1 State Space Model

We recall from Chapter 3 that (3.9) is the model equation of the VSC and we represent it in a state space control affine form as the following.

$$\dot{x} = f(x) + g_1(x)u_1 + g_2(x)u_2, \tag{4.1}$$

where

$$x = (x_1, x_2, x_3)^T = (i_d, i_q, v_{dc})^T$$
$$u = (u_1, u_2)^T = (m_a \cos\delta, m_a \sin\delta)^T$$

with

$$f(x) = \begin{bmatrix} -\frac{R_s}{L}x_1 + \omega x_2 + \frac{v_d}{L} \\ -\omega x_1 - \frac{R_s}{L}x_2 \\ -\frac{x_3}{CR_c} \end{bmatrix}$$

and

$$g_1(x) = \begin{bmatrix} -\frac{x_3}{2L} \\ 0 \\ \frac{3x_1}{4C} \end{bmatrix}, \quad g_2(x) = \begin{bmatrix} 0 \\ -\frac{x_3}{2L} \\ \frac{3x_2}{4C} \end{bmatrix}.$$

Since m_a and δ are bounded, i.e

$$0 \le m_a \le 1, \quad -\frac{\pi}{2} \le \delta \le \frac{\pi}{2}$$

the inputs u_1 and u_2 are also bounded by

$$0 \le u_1 \le 1, \quad u_1^2 + u_2^2 \le 1.$$

It is also desired to give boundaries for the three states since currents and voltages must be limited to the rated values. For the experimental setup of the VSC we require

$$-20 \text{ A} \le x_1 \le 20 \text{ A}$$
$$-20 \text{ A} \le x_2 \le 20 \text{ A}$$
$$0 \text{ V} < x_3 \le 600 \text{ V}.$$

We also note that although DC voltage can be negative, most VSC applications assume x_3 to be strictly positive.

4.2 Equilibrium Set of the System

Our control objective is to steer the VSC between constant operating points, i.e., between points in the equilibrium set. Here we define the equilibrium set as the following.

Definition 4.2.1 *An equilibrium set of the nonlinear system* (4.1) *is a set*

$$\{x \in \mathbb{R}^3 : f(x) + u_1 g_1(x) + u_2 g_2(x) = 0, u_1, u_2 \text{ const.}\}.$$

In other words, once the system reaches an equilibrium point, the states will remain unchanged as long as the control input is unchanged. Applying this definition to the system, we have

$$\begin{aligned} -\frac{R_s}{L}x_{10} + \omega x_{20} + \frac{v_d}{L} - \frac{1}{2L}x_{30}u_{10} &= 0 \\ -\omega x_{10} - \frac{R_s}{L}x_{20} - \frac{1}{2L}x_{30}u_{20} &= 0 \\ \frac{3(x_{10}u_{10} + x_{20}u_{20})}{4C} - \frac{x_{30}}{CR_c} &= 0 \end{aligned} \tag{4.2}$$

where x_{10}, x_{20}, x_{30} are the equilibrium state and u_{10}, u_{20} are constants. Now solving (4.2) for the equilibrium state in terms of the system input gives

$$\begin{aligned} x_{10} &= \frac{v_d(8R_s + 3R_c u_{20}^2)}{8R_s^2 + 3R_s R_c u_{10}^2 + 3R_c u_{20}^2 R_s + 8L^2\omega^2} \\ x_{20} &= -\frac{v_d(8L\omega + 3R_c u_{10}u_{20})}{8R_s^2 + 3R_s R_c u_{10}^2 + 3R_s R_c u_{20}^2 + 8L^2\omega^2} \\ x_{30} &= \frac{6R_c v_d(R_s u_{10} - u_{20}L\omega)}{8R_s^2 + 3R_s R_c u_{10}^2 + 3R_s R_c u_{20}^2 + 8L^2\omega^2}. \end{aligned} \tag{4.3}$$

Based on the voltage and current ratings of the system, a subset of the equilibrium values of (4.3) is shown in Figure 4.1 and Figure 4.2. The parameters used for evaluating the equilibrium are the actual system parameters of the experimental setup shown in Table 3.1. Figure 4.2 shows the equilibrium values of i_d and i_q as a function of δ with $m_a = 0.8$. Only variation in δ is shown as the currents have little dependence on m_a. Figure 4.1 and 4.2 illustrate that as δ increases both i_q and v_{dc} decrease. An increase in m_a leads to a noticeable decrease in only v_{dc} while i_d and i_q remain relatively constant.

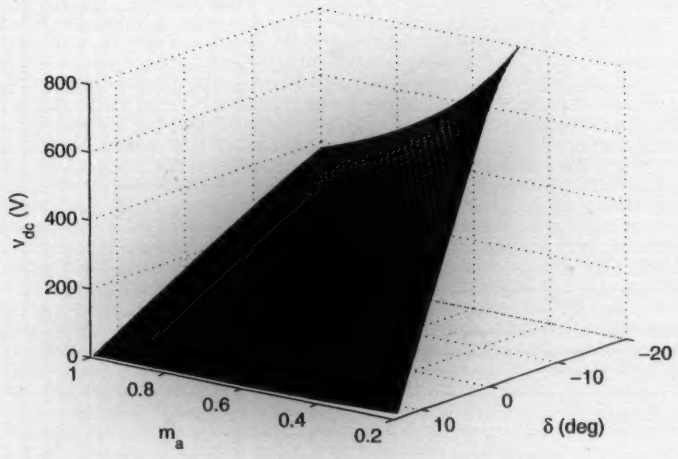


Figure 4.1: Equilibrium values of v_{dc}

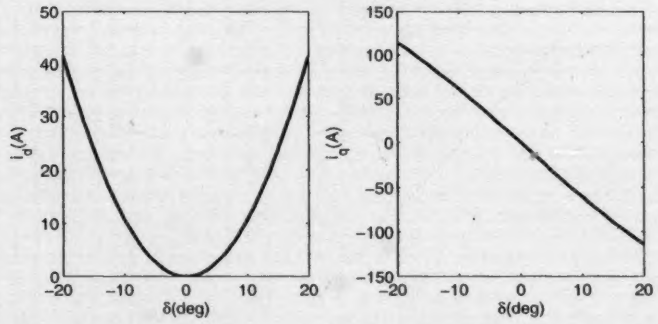


Figure 4.2: Equilibrium values of i_d and i_q as a function of δ

4.3 Feedback Linearization

The theory of nonlinear feedback linearization is well documented in [13], [28], and in [20]. Here we adopt the notation and procedures of multi-input feedback linearization described in [20]. In this section, the objective is to apply feedback linearization technique in order to test whether the conditions for feedback linearizability are satisfied for this particular VSC system under consideration. Loosely speaking, feedback linearization is a technique where the nonlinear system can be linearized in a new system with a linearizing state

feedback. Not all systems are feedback linearizable hence we state the conditions for feedback linearizability for multi-input systems. First, we require the definition of controllability indices. Refer to Appendix A for standard notation and definitions from differential geometry.

Definition 4.3.1 *For an n-state m-input nonlinear system*

$$\dot{x} = f(x) + \sum_{i=1}^{m} g_i(x)u_i, \quad x \in \mathbb{R}^n, \tag{4.4}$$

the controllability indices $\{k_1, \ldots, k_m\}$ *are defined as*

$$k_i = card\{m_j \geq i : j \geq 0\}, \quad 1 \leq i \leq m,$$

where

$$\begin{aligned} m_0 &= rank\ \mathcal{G}_0 \\ m_1 &= rank\ \mathcal{G}_1 - rank\ \mathcal{G}_0 \\ &= \vdots \\ m_{n-1} &= rank\ \mathcal{G}_{n-1} - rank\ \mathcal{G}_{n-2}. \end{aligned}$$

with

$$\mathcal{G}_i = span\{g_1, \ldots, g_m, \ldots, ad_f^i g_1, \ldots, ad_f^i g_m\}, \quad 0 \leq i \leq n-1.$$

Note that the cardinality of the set denoted *card* is the number of elements in the set. With this definition the following theorem describes the conditions for the Local State FeedBack Linearization (LSFBL).

Theorem 4.3.1 *The nonlinear system (4.4) is locally transformable in a neighborhood of an equilibrium point* x_o *by a nonsingular state feedback transformation (which consists of a nonsingular state feedback and a diffeomorphism) into a linear controllable system in Brunovsky controller form with controllability indices* $k_1 \geq \ldots \geq k_m$ *if, and only if, in a neighborhood of* x_o*:*

1. *The distributions* $\mathcal{G}_{k_i-2}$, $1 \leq i \leq m$ *are involutive and of constant rank.*
2. *rank* $\mathcal{G}_{k_1-1} = n$.

Now we apply the above theorem to the system (4.1). To check the above conditions, the distributions $\mathcal{G}_0$, $\mathcal{G}_1$ are first constructed in matrix format and then the controllability indices are determined. The matrix form of $\mathcal{G}_0$, $\mathcal{G}_1$ denoted G_0, G_1, respectively, are

$$G_0 = \begin{bmatrix} -\frac{x_3}{2L} & 0 \\ 0 & -\frac{x_3}{2L} \\ \frac{3x_1}{4C} & \frac{3x_2}{4C} \end{bmatrix}$$

$$G_1 = \begin{bmatrix} -\frac{x_3}{2L} & 0 & \frac{(L-CR_cR_s)x_3}{2CL^2R_c} & \frac{x_3\omega}{2L} \\ 0 & -\frac{x_3}{2L} & -\frac{x_3\omega}{2L} & \frac{(L-CR_cR_s)x_3}{2CL^2R_c} \\ \frac{3x_1}{4C} & \frac{3x_2}{4C} & \frac{3(Lx_1+CR_c(v_d-R_sx_1+Lx_2\omega))}{4C^2LR_c} & \frac{3(-Lx_2+CR_cR_sx_2+CLR_cx_1\omega)}{4C^2LR_c} \end{bmatrix}.$$

Since v_{dc} is assumed to be positive, $x_3 > 0$. Therefore,

$$m_0 = rank\ G_0 = 2$$

In order to find the rank of G_1, we do the following row reduction.

$$\begin{aligned} r_1' &= r_1 \cdot -\frac{2L}{x_3} \\ r_2' &= r_2 \cdot -\frac{2L}{x_3} \\ r_3' &= r_3 - r_1' \cdot \frac{3x_1}{4C} \\ r_3'' &= r_3' - r_2' \cdot \frac{3x_2}{4C} \end{aligned}$$

where r_1, r_2, r_3 are the rows of G_1 as the following.

$$G_1 = \begin{bmatrix} r_1 \\ r_2 \\ r_3 \end{bmatrix}$$

Then the row reduced form of G_1 is

$$G_{1,r} = \begin{bmatrix} r_1' \\ r_2' \\ r_3'' \end{bmatrix} = \begin{bmatrix} 1 & 0 & -\frac{1}{CR_c} + \frac{R_s}{L} & -\omega \\ 0 & 1 & \omega & -\frac{1}{CR_c} + \frac{R_s}{L} \\ 0 & 0 & \frac{6Lx_1+3CR_c(v_d-2R_sx_1)}{4C^2LR_c} & \frac{3(L-CR_cR_s)x_2}{2C^2LR_c} \end{bmatrix}$$

Therefore the rank of G_1 is 3 except when either

$$\bar{x}_1 = \frac{CR_cv_d}{2(CR_cR_s - L)} \text{ and } \bar{x}_2 = 0, \text{ or } \bar{x}_3 = 0.$$

However, in practice the current $\bar{x}_1$ is far from any realistic operating condition and therefore does not limit the domain on which the rank of G_1 is 3. For example, substituting parameters from Table 3.1 gives $\bar{x}_1 = 177.52$ A, and we require that current amplitude not exceed 20 A. Therefore we conclude that

$$m_1 = rank\ G_1 - rank\ G_0 = 1$$

and the controllability indices are

$$k_1 = 2, \quad k_2 = 1.$$

So far we have shown that G_0 and G_1 are of constant rank and that the rank of G_1 is 3 in the region $\mathbf{S}$ which we define as the following for convenience:

$$\mathbf{S} = \{x \in \mathbb{R}^3 : x_1 < \bar{x}_1; x_3 > 0\}. \tag{4.5}$$

We can also show that G_0 is involutive since the Lie bracket of vector fields g_1 and g_2 gives

$$\begin{aligned} ad_{g_1} g_2 &= \frac{3x_2}{8LC}\frac{\partial}{\partial x_1} - \frac{3x_1}{8LC}\frac{\partial}{\partial x_2} \\ &= \frac{-3x_2}{8Cx_3} g_1 + \frac{3x_1}{8Cx_3} g_2 \end{aligned}$$

which is a linear combination of g_1 and g_2.

Therefore, we conclude that the conditions described in Theorem 4.3.1 are satisfied for the nonlinear VSC model (4.1) and hence, it is locally state feedback linearizable. Theorem 4.3.1 also guarantees the existence of smooth functions $\phi_k : \mathbb{R}^n \to \mathbb{R}$, $k = 1, \ldots, m$, such that the diffeomorphism defined as

$$\begin{bmatrix} z_1 \\ \vdots \\ z_n \end{bmatrix} = \begin{bmatrix} \phi_1 \\ \vdots \\ L_f^{k_1-1}\phi_1 \\ \vdots \\ \phi_m \\ \vdots \\ L_f^{k_m-1}\phi_m \end{bmatrix}$$

and the linearizing state feedback defined as

$$w = \begin{bmatrix} L_f^{k_1}\phi_1 \\ \vdots \\ L_f^{k_m}\phi_m \end{bmatrix} + \begin{bmatrix} L_{g_1}L_f^{k_1-1}\phi_1 & \ldots & L_{g_m}L_f^{k_1-1}\phi_1 \\ \vdots & \ddots & \vdots \\ L_{g_1}L_f^{k_m-1}\phi_m & \ldots & L_{g_m}L_f^{k_m-1}\phi_m \end{bmatrix} \begin{bmatrix} u_1 \\ \vdots \\ u_m \end{bmatrix}$$

will linearize the system in the neighborhood of some equilibrium point x_o in region **S**. For the VSC model we have

$$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} \phi_1 \\ L_f\phi_1 \\ \phi_2 \end{bmatrix}.$$

Taking the time derivative of the z's gives the dynamics of the system in z-coordinates as the following.

$$\begin{aligned}
\dot{z}_1 &= \frac{\partial \phi_1}{\partial x}\dot{x} = L_f\phi_1 + L_{g_1}\phi_1 u_1 + L_{g_2}\phi_1 u_2 \\
\dot{z}_2 &= \frac{\partial L_f\phi_1}{\partial x}\dot{x} = L_f^2\phi_1 + L_{g_1}L_f\phi_1 u_1 + L_{g_2}L_f\phi_1 u_2 \\
\dot{z}_3 &= \frac{\partial \phi_2}{\partial x}\dot{x} = L_f\phi_2 + L_{g_1}\phi_2 u_1 + L_{g_2}\phi_2 u_2
\end{aligned}$$

or, in matrix form,

$$\frac{d}{dt}\begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} L_f\phi_1 \\ L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + \begin{bmatrix} L_{g_1}\phi_1 & L_{g_2}\phi_1 \\ L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}.$$

Here we choose ϕ_1 such that $\phi_1 \in \mathcal{G}_0^{\perp}$, i.e., $< \mathrm{d}\phi_1, g_k >= 0,\ k = 1, 2$. This ensures that

$$L_{g_1}\phi_1 = 0, \quad L_{g_2}\phi_1 = 0 \tag{4.6}$$

and therefore

$$\frac{d}{dt}\begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} L_f\phi_1 \\ L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}. \tag{4.7}$$

The only condition for choosing ϕ_2 is that

$$F = \begin{bmatrix} L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix} \tag{4.8}$$

be nonsingular in a neighborhood of some equilibrium point x_o in **S**. Then it follows that the matrix F is invertible and defining the control inputs as

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = F^{-1}\begin{bmatrix} w_1 - L_f^2\phi_1 \\ w_2 - L_f\phi_2 \end{bmatrix}$$

gives

$$\begin{aligned}
\dot{z}_1 &= z_2 \\
\dot{z}_2 &= w_1 \\
\dot{z}_3 &= w_2
\end{aligned}$$

where we have chosen ϕ_2 such that F^{-1} exists. Now w_1 and w_2 can be designed using linear system techniques such as pole placement or LQR. For example, if we choose

$$w_1 = -k_1 z_1 - k_2 z_2$$
$$w_2 = -k_3 z_3$$

with $k_i > 0,\ i = 1, 2, 3$, then we have

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -k_1 & -k_2 & 0 \\ 0 & 0 & -k_3 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix}$$

which is a stable system.

4.3.1 Finding ϕ_1 and ϕ_2

To simplify the notation, we represent G_0 and G_1 as

$$G_0 = \begin{bmatrix} G_{011} & 0 \\ 0 & G_{011} \\ G_{031} & G_{032} \end{bmatrix}, \quad G_1 = \begin{bmatrix} G_{011} & 0 & G_{113} & G_{114} \\ 0 & G_{011} & G_{123} & G_{124} \\ G_{031} & G_{032} & G_{133} & G_{134} \end{bmatrix}.$$

From (4.6), ϕ_1 must satisfy

$$\frac{\partial \phi_1}{\partial x} g_1 = \frac{\partial \phi_1}{\partial x_1} G_{011} + \frac{\partial \phi_1}{\partial x_3} G_{031} = 0$$
$$\frac{\partial \phi_1}{\partial x} g_2 = \frac{\partial \phi_1}{\partial x_2} G_{011} + \frac{\partial \phi_1}{\partial x_3} G_{032} = 0.$$

Solving the above partial differential equations using Maple's `pdesolve` we obtain the following general solution.

$$\phi_1(x) = \psi\left(\frac{3L}{2C}(x_1^2 + x_2^2) + x_3^2\right) + c \tag{4.9}$$

where ψ is some C^1 function, and c is some constant. A physically relevant choice for ϕ_1 is the total energy stored in the inductors (E_L) and the capacitor (E_C)

$$E_L = \frac{1}{2} L(i_a^2 + i_b^2 + i_c^2) = \frac{3}{4} L(i_d^2 + i_q^2)$$
$$E_C = \frac{1}{2} C v_{dc}^2$$

and hence, we choose

$$\phi_1(x) = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3^2.$$

The only condition on choosing ϕ_2 is that the matrix $F(x)$ be nonsingular about x_0. A simple choice is $\phi_2(x) = x_2$ which allows us to track the reactive current i_q. With ϕ_1 and ϕ_2 chosen this way, the resulting matrix $F(x)$ is

$$F(x) = \begin{bmatrix} -\frac{3x_3(2Lx_1+CR_c(v_d-2R_sx_1))}{R_cLC^2} & -\frac{6x_2x_3(L-CR_cR_s)}{C^2LR_c} \\ 0 & -\frac{x_3}{L} \end{bmatrix}$$

which is nonsingular in the region **S** as defined in (4.5).

4.4 Flatness-based Control Design

The relation between feedback linearization and flatness is well known [22]. In this section we make use of both notions as system (4.1) is locally static state feedback linearizable. Being static state feedback linearizable allows us to systematically determine a flat output. Flatness is then used to design an open-loop control which steers the system between equilibrium points while respecting constraints on the input. We remark that work in [9, 10] presented a similar flat output but omitted its derivation. In the last section, we have explicitly computed the PDE and its solution to determine the linearizing coordinate transformation which is the flat output. The reason that the flat output can be chosen in this way is because the system is static state feedback linearizable which enables us to choose the flat output as the lead components of the linearizing coordinates i.e., ϕ_1 and ϕ_2. It is interesting to remark that any $(m+1)$-dimensional system with m-inputs is flat if, and only if it is controllable [5]. Since the VSC is a 3-state 2-input system and is controllable, it is necessarily flat.

4.4.1 Differential Flatness

Before proceeding with the flatness-based control design, we give a definition of flatness.

Definition 4.4.1 *The control system*

$$\dot{x} = f(x, u), \quad x \in \mathbb{R}^n, \quad u \in \mathbb{R}^m$$

is said to be differentially flat (or simply flat) if there exists smooth maps h, $\mathcal{A}$, $\mathcal{B}$ such that

$$y = h(x, \dot{u}, \cdots, u^{(\rho)})$$
$$x = \mathcal{A}(y, \dot{y}, \cdots, y^{(r)})$$
$$u = \mathcal{B}(y, \dot{y}, \cdots, y^{(r+1)})$$

where ρ and r are some positive integers and the components of y are not related by a differential relation of the form

$$P(y, \dot{y}, \ddot{y}, \cdots, y^{(r+1)}) = 0.$$

In other words, a system with m inputs is flat if there exists m output functions $f_1, \cdots, f_m$ called *flat outputs* that can explicitly parameterize the states x and inputs u. This implies that if the flat output values are known, we can determine the values of the states and inputs by a smooth mapping i.e., without integration. This is particularly interesting property for open loop trajectory planning since by planning the trajectory of the flat outputs, we can determine the input trajectory that will steer the system from one equilibrium state to another desired equilibrium state.

4.4.2 Flat Output and Open-loop Motion Planning

In static state feedback linearizable systems, the flat outputs are the lead components of the coordinate transformation for each input, i.e.,

$$y_1(x) = \phi_1(x) = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3^2 \tag{4.10}$$
$$y_2(x) = \phi_2(x) = x_2 \tag{4.11}$$

where y_1, y_2 denote the components of the flat output. The time derivative of y_1 is

$$\dot{y}_1 = L_f\phi_1(x) = \frac{3R_c(v_d x_1 - R_s(x_1^2 + x_2^2)) - 2x_3^2}{2R_c} \tag{4.12}$$

From (4.10) and (4.12), we can express the states x_1, x_2, x_3 in terms of $y_1, \dot{y}_1, y_2$.

$$\begin{aligned} x_1 &= \frac{3CR_c v_d - \psi(y,\dot{y})}{6(CR_cR_s - L)} \\ x_2 &= y_2 \\ x_3 &= \frac{\sqrt{R_c\zeta(y,\dot{y}) - LR_c(8R_s y_1 + 4L\dot{y}_1 - v_d\psi(y))}}{2(CR_cR_s - L)} \end{aligned} \tag{4.13}$$

where

$$\psi(y,\dot{y}) = \sqrt{9C^2R_c^2v_d^2 + 12\sigma(4y_1 + 2CR_c\dot{y}_1 - 3\sigma y_2^2)}$$

with $\sigma = L - CR_cR_s$ and

$$\zeta(y,\dot{y}) = CR_c(-3Lv_d^2 + 8R_s^2y_1 + 4LR_s\dot{y}_1).$$

The inputs u_1, u_2 can be expressed in terms of $y_1, \dot{y}_1, \ddot{y}_1, y_2$, and $\dot{y}_2$. From (4.7), we have

$$\dot{y}_1 = y_2$$

with

$$\begin{bmatrix} \ddot{y}_1 \\ \dot{y}_2 \end{bmatrix} = \begin{bmatrix} L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + F \begin{bmatrix} u_1 \\ u_2 \end{bmatrix},$$

and solving the above equations for u_1 and u_2 gives

$$\begin{aligned} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} =& F^{-1}(x) \begin{bmatrix} \ddot{y}_1 - L_f^2\phi_1(x) \\ \dot{y}_2 - L_f\phi_2(x) \end{bmatrix} \\ =& \begin{bmatrix} \frac{4CLR_c}{-3CR_cv_dx_3 - 6Lx_1x_3 + 6CR_cR_sx_1x_3} & \frac{4L(L-CR_cR_s)x_2}{(2Lx_1 + CR_c(v_d - 2R_sx_1))x_3} \\ 0 & -\frac{2L}{x_3} \end{bmatrix} \\ & \begin{bmatrix} \ddot{y}_1 - \frac{3(v_d^2 + v_d(-3R_sx_1 + \omega Lx_2) + 2R_s^2(x_1^2 + x_2^2))}{2L} - \frac{2x_3^2}{CR_c^2} \\ \dot{y}_2 + \omega x_1 + \frac{R_s}{L}x_2 \end{bmatrix}, \end{aligned}$$

and replacing the x's with their proper expressions in terms of y's gives the final expressions for u_1 and u_2 as functions of the flat outputs. This rather complicated expressions for x and u can be simplified by assuming a lossless system with $R_s = 0$ and $R_c = \infty$. In this case, the expressions for the state and input are much simpler:

$$\begin{aligned} x_1 &= \frac{2\dot{y}_1}{3v_d} \\ x_2 &= y_2 \\ x_3 &= \sqrt{\frac{2}{C}y_1 - \frac{2L\dot{y}_1^2}{3Cv_d^2} - \frac{3L}{2C}y_2^2} \end{aligned}$$

and

$$u_1 = \frac{-\frac{4L}{3v_d}\ddot{y}_1 + 2(v_d + \omega L y_2)}{\sqrt{\frac{2}{C}y_1 - \frac{2L\dot{y}_1^2}{3Cv_d^2} - \frac{3L}{2C}y_2^2}}$$

$$u_2 = -\frac{2L\dot{y}_2 + \frac{4\omega L}{3v_d}\dot{y}_1}{\sqrt{\frac{2}{C}y_1 - \frac{2L\dot{y}_1^2}{3Cv_d^2} - \frac{3L}{2C}y_2^2}}.$$

We remark that the flat outputs are closely related to the variables we want to influence i.e., i_q and v_{dc}. This is because energy stored in the capacitor is much larger than that in the inductors. Hence, tracking energy is similar to tracking v_{dc}.

Using the above simplified expressions, we proceed with the open loop motion planning. The desired flat output trajectories are designed to determine an open loop control which steers the system between equilibria at $t = t_0$ and $t = t_1 > t_0$ while meeting certain constraints. To illustrate this design we choose a specific motion planning problem:

1. $i_q(t_0) = -10$ A, $i_q(t_1) = 10$ A.
2. $v_{dc}(t_0) = 200$ V, $v_{dc}(t_1) = 240$ V.
3. Inputs m_a and δ must satisfy

$$0 \leq m_a(t) \leq 1, -\frac{\pi}{2} \leq \delta(t) \leq \frac{\pi}{2}, \quad t_0 \leq t \leq t_1.$$

4. The currents must satisfy

$$-20 \text{ A} \leq i_d(t) \leq 20 \text{ A}, \ -20 \text{ A} \leq i_q \leq 20 \text{ A}, \ t_0 \leq t \leq t_1.$$

The transition time is chosen to be 50 ms. We remark that the real current i_d is necessarily 0 at equilibrium points. Also, the transition time $\Delta t = t_1 - t_0$ should be as small as possible. To ensure that objectives 3 and 4 are satisfied, the flat outputs are parameterized with a polynomial basis and the coefficients of this parametrization are optimized. This optimization is performed numerically using MATLAB's `fseminf`. The MATLAB code for this optimization

process is included in Appendix B. The resulting polynomials are

$$y_{1,d}(t) = 66.188 + 1.4 \times 10^7 t^3 - 1.7 \times 10^9 t^4 + 6.7 \times 10^{10} t^5$$
$$y_{2,d}(t) = -10 + 48000t^2 - 1920000t^3$$

where $t_0 = 0$ and $t_1 = 50$ ms. The subscript d represents the *desired* trajectory. We remark that the end points of the polynomials have the following values.

$$y_{1,d}(t_0) = \frac{1}{2}(0.0033)(200)^2 + \frac{3}{4}(0.0025)(-10)^2 = 66.1875$$
$$y_{1,d}(t_1) = \frac{1}{2}(0.0033)(240)^2 + \frac{3}{4}(0.0025)(10)^2 = 95.2275$$
$$y_{2,d}(t_o) = -10$$
$$y_{2,d}(t_1) = 10.$$

The graphs shown in Figure 4.3 are the polynomials $y_{1,d}$ and $y_{2,d}$ where $t_0 =$ 1 s, and $t_1 = 1.05$ s. Figure 4.4 is the waveform of the corresponding inputs m_a and δ.

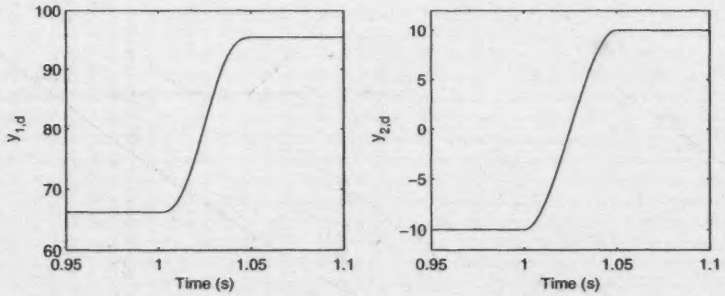


Figure 4.3: Desired trajectories of $y_{1,d}, y_{2,d}$

4.4.3 Flatness-based Closed-loop Trajectory Tracking

In ideal case, the open-loop trajectory control should be able to drive the system from one equilibrium point to another, but in practice, due to the unknown disturbances and modeling error, open-loop control is not sufficient to steer the system to the exact desired state. To account for disturbances, model error, and initial tracking error, open-loop control is augmented with

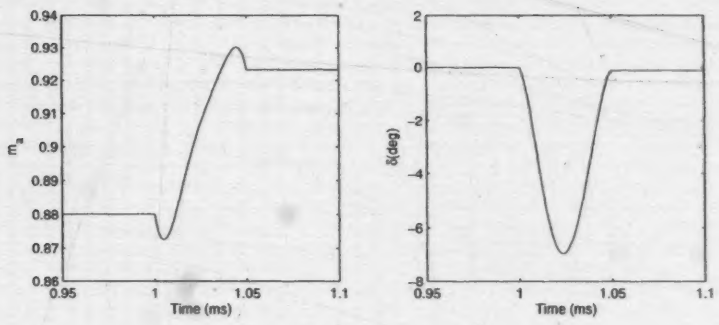


Figure 4.4: Input trajectories m_a and δ

state feedback. We define the components of the tracking error as

$$
\begin{aligned}
e_1(t) &= \int_0^t (y_1(\tau) - y_{1,d}(\tau))d\tau \\
e_2(t) &= y_1(t) - y_{1,d}(t) \\
e_3(t) &= \frac{dy_1}{dt}(t) - \frac{dy_{1,d}}{dt}(t) \\
e_4(t) &= \int_0^t (y_2(\tau) - y_{2,d}(\tau))d\tau \\
e_5(t) &= y_2(t) - y_{2,d}(t)
\end{aligned}
$$

where $y_{1,d}$ and $y_{2,d}$ are the desired flat outputs designed in the previous section. Then we have

$$
\begin{aligned}
\dot{e}_1 &= e_2 \\
\dot{e}_2 &= e_3 \\
\dot{e}_3 &= \ddot{y}_1 - \ddot{y}_{1,d} = L_f^2\phi_1 + L_{g_1}L_f\phi_1 u_1 + L_{g_2}L_f\phi_1 u_2 - \ddot{y}_{1,d} \\
\dot{e}_4 &= e_5 \\
\dot{e}_5 &= \dot{y}_2 - \dot{y}_{2,d} = L_f\phi_2 + L_{g_1}\phi_2 u_1 + L_{g_2}\phi_2 u_2 - \dot{y}_{2,d}.
\end{aligned}
$$

Hence, taking

$$
\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = F^{-1}(x) \begin{bmatrix} -k_1e_1 - k_2e_2 - k_3e_3 - L_f^2\phi_1 + \ddot{y}_{1,d} \\ -k_4e_4 - k_5e_5 - L_f\phi_2 + \dot{y}_{2,d} \end{bmatrix}
$$

gives linear error dynamics

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \\ \dot{e}_4 \\ \dot{e}_5 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -k_1 & -k_2 & -k_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -k_4 & -k_5 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \end{bmatrix}.$$

The integral of the tracking error is included to reject the effects of constant disturbances. Fig. 4.5 illustrates the block diagram of the flatness-based closed-loop control.

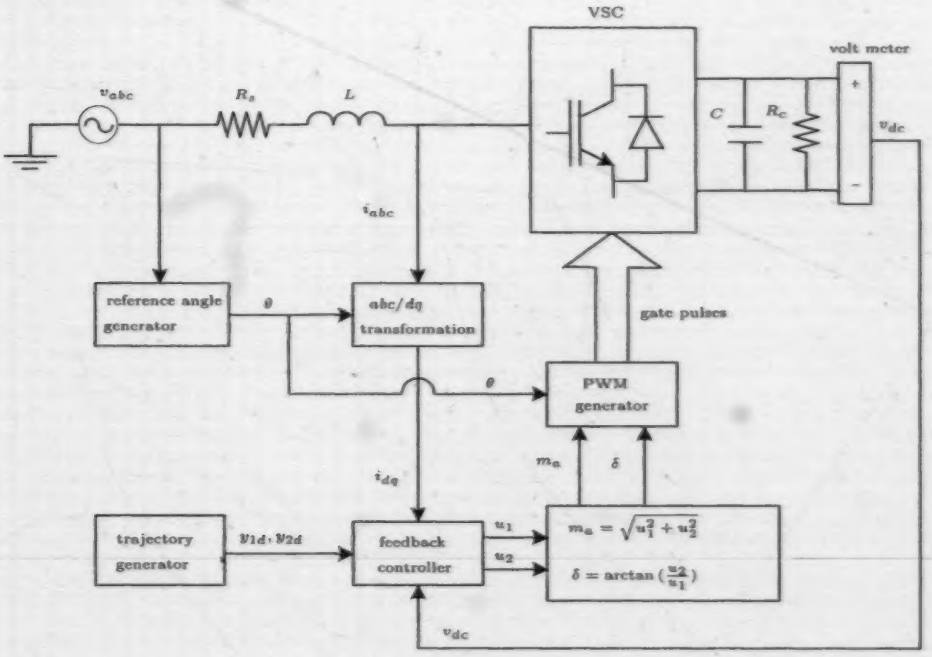


Figure 4.5: Flatness-based control scheme

4.5 Simulation Results

In this section, a simulation of the flatness-based control technique for a VSC system is presented. This simulation is performed on MATLAB/Simulink where the plant consists of the model equations for VSC in d-q frame, the inputs to the plant are m_a, δ and the outputs from the plant are the three

states i.e., i_d, i_q, v_{dc}. The trajectory generator sends the parameterized flat output which is designed to meet the control objectives and constraints. The transition of states is designed to occur at $t = 1$ s. In order to verify that the closed-loop state feedback control is working properly, the initial state of the system is at $(x_1, x_2, x_3) = (0, 0, 200)$ which is slightly away from the desired equilibrium points. The feedback gains used in this simulation are $k_1 = 8500\ \text{s}^{-3}, k_2 = 5600\ \text{s}^{-2}, k_3 = 100\ \text{s}^{-1}, k_4 = 2800\ \text{s}^{-2}, k_5 = 150\ \text{s}^{-1}$.

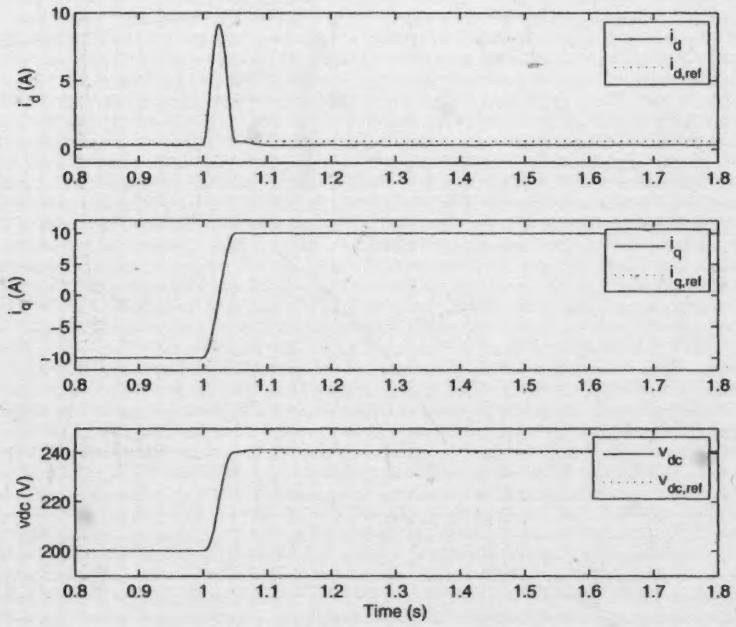


Figure 4.6: Simulation results of i_d, i_q, v_dc.

Figure 4.6 shows the transition of the three states between $t = 1$ s and $t = 1.05$ s and Figure 4.7 shows the corresponding control inputs m_a and δ. The simulation shows that all three states closely follow the desired trajectory. We note that the expression for the controller is simplified for the case when $R_s = 0$ and $R_c = \infty$ in order to reduce the complexity of the equation, and this may be the reason for the discrepancy between the desired trajectory and the actual values of the states.

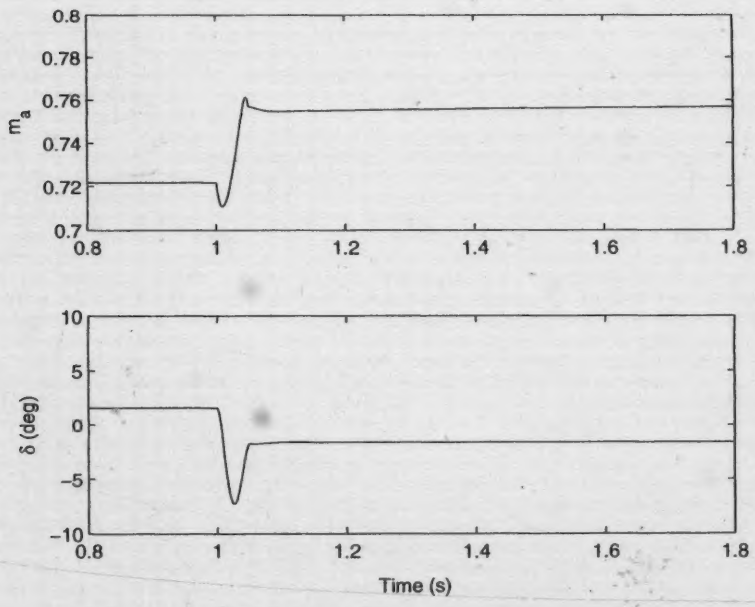


Figure 4.7: Simulation results of the control inputs m_a, δ.

4.6 Decoupled Vector Control Scheme

In order to evaluate the performance of the flatness-based control, a traditional vector control method presented in [26] is briefly reviewed in this section. We recall the two current equations in d-q frame from (3.7) which are

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + \omega i_q + \frac{v_d}{L} - \frac{e_d}{L} \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q - \omega i_d - \frac{e_q}{L}. \end{aligned} \tag{4.14}$$

Now we define e_d and e_q as the following.

$$\begin{aligned} e_d &= v_d + L(\omega i_q - p_1) \\ e_q &= L(-\omega i_d - p_2) \end{aligned} \tag{4.15}$$

where p_1, p_2 are the outputs from the PI compensators of i_d and i_q, respectively. Substituting (4.15) into (4.14) gives

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + p_1 \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q + p_2. \end{aligned}$$

Hence we can independently control both i_d and i_q, and there's no cross-coupling between them. The PI feedback is

$$p_1 = k_{id}^p(i_d^* - i_d) + k_{id}^i \int_0^\tau (i_d^* - i_d)d\tau$$
$$p_2 = k_{iq}^p(i_q^* - i_q) + k_{iq}^i \int_0^\tau (i_q^* - i_q)d\tau$$

or in frequency domain

$$P_1(s) = \left(k_{id}^p + \frac{k_{id}^i}{s}\right)(I_d^* - I_d)$$
$$P_2(s) = \left(k_{iq}^p + \frac{k_{iq}^i}{s}\right)(I_q^* - I_q).$$

Since the DC voltage in the capacitor is related to the amount of real current entering the VSC, the DC voltage is indirectly controlled by controlling the real current i.e., i_d. Therefore the output of the PI compensator for the DC voltage is i_d^* i.e.,

$$I_d^*(s) = \left(k_v^p + \frac{k_v^i}{s}\right)(V_{dc}^* - V_{dc})$$

This control scheme results in cascaded PI compensators for v_{dc} and i_d where the *inner feedback loop* is the i_d controller and the *outer feedback loop* is the v_{dc} controller. This type of control scheme is also known as an *inner-outer loop control*. The i_q control has only one PI compensator and is independent of i_d and v_{dc}.

We remark that the response time of the inner loop control should be much faster than that of the outer loop control in order for the cascaded PI loop to work properly. We also note that in the VSC system, the AC currents respond almost instantaneously to the step change in inputs (i.e., m_a, δ) whereas the speed at which the DC capacitor bank charges is relatively slow. Hence the inner-outer loop control scheme is appropriate for the i_d and v_{dc} control. Figure 4.8 illustrates a block diagram of this controller.

4.7 Summary

In this chapter, we have derived the set of equilibrium and have shown that the VSC system is static state feedback linearizable. A flatness-based control

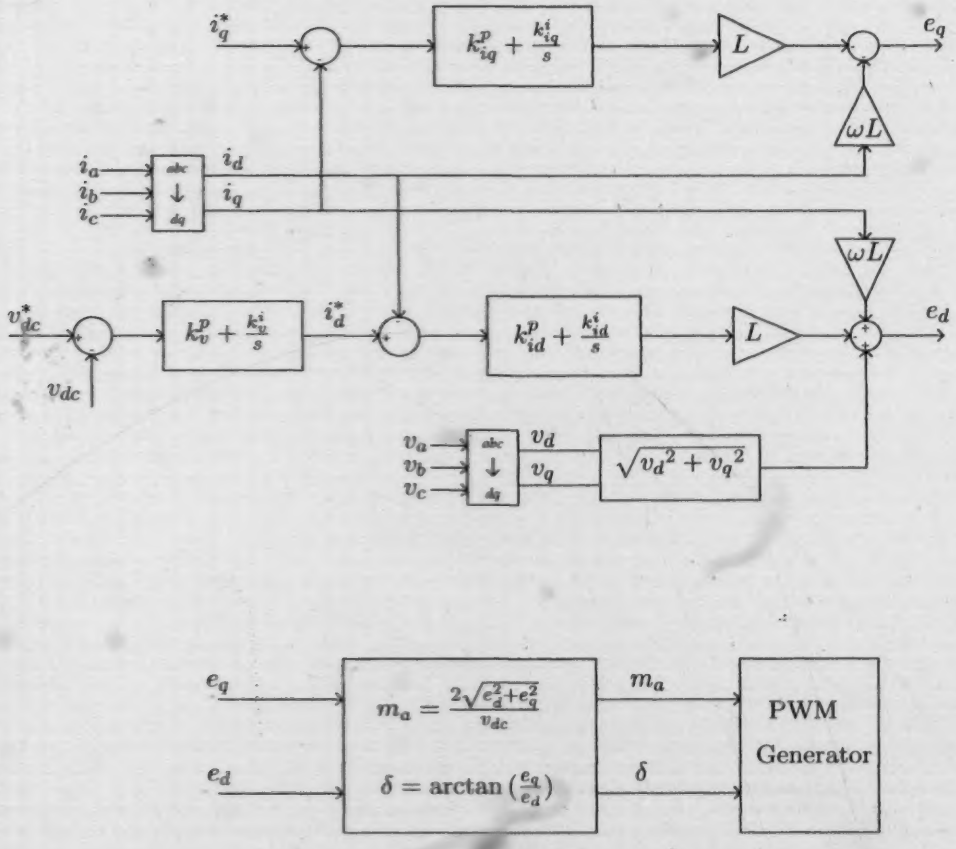


Figure 4.8: Block diagram of vector control scheme.

has also been implemented, and the open-loop motion planning is used to steer the system between equilibria while respecting the input and state constraints. This control scheme is implemented in simulation and the results show that open-loop motion planning combined with closed-loop control ensures robust tracking control.

Chapter 5

Experimental Verification

This chapter presents the design and implementation of the VSC control system on an experimental setup to validate the theory presented in Chapter 4. The VSC used in the experiment is the PowerPak IGBT-based 3-phase inverter [1], and the control algorithm is implemented in real-time digital simulator manufactured by Opal-RT Technologies [2]. The simulator contains a Xilinx Virtex II Pro FPGA [3] card which is used to generate the sine PWM gating pulses. The simulator also contains a high speed analog-to-digital and digital-to-analog converters as well as digital input and output boards. The experiment is performed at a sampling rate of 4 kHz with carrier frequency of 2 kHz. It is also possible to have the same sampling frequency as the carrier frequency, but the mathematical model of the system does not change in either case and it is expected that having faster sampling frequency will result in better performance. All the experiments are done in the Real-Time eXperimental LAB (RTX-LAB) at the University of Alberta.

5.1 Experimental Setup

5.1.1 The 6-pulse VSC

Figure 5.1 shows a VSC assembled by Powerex rated at 1.5 kVA (model number: PP75T120). The converter consists of 6 Insulated Gate Bipolar Transistors (IGBTs) manufactured by Applied Power Systems Inc. The gate drive board is mounted on the top of the converter and is responsible for sending the 6 digital gating signals as well as for measuring various signals including

heat sink temperature, three-phase currents, and DC voltage. The gate drive board also contains security features such as over-current detection and 2 μs of dead-time.

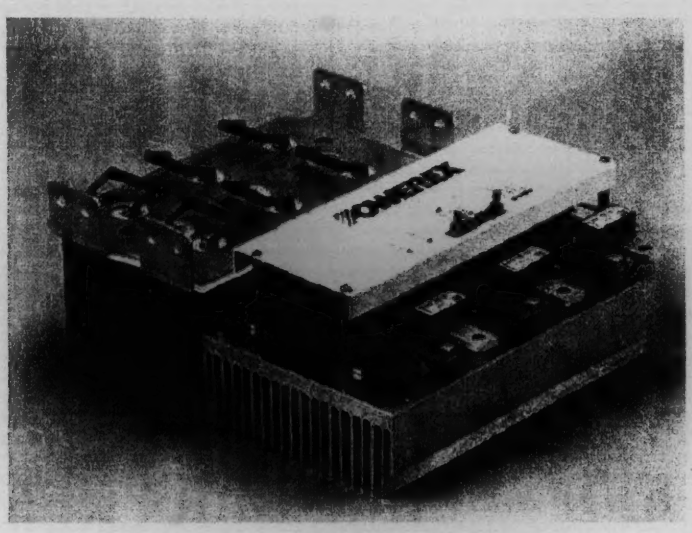


Figure 5.1: 6-pulse IGBT-based VSC

5.1.2 Real-time Digital Simulator

For computing the control algorithm the real-time digital simulator manufactured by Opal-RT Technologies is used and it provides an enormous amount of computing power which is suitable for calculating advanced control schemes or performing hardware-in-the-loop simulation. Figure 5.2 shows the real-time simulator manufactured by Opal-RT Technologies Inc. Each tower contains 4 computing units called *nodes* and each node houses 2 Intel Xeon processors, analog-to-digital and digital-to-analog converters, and digital input/output cards. In our work only one node is required. The node used for the experiment also houses a Xilinx Virtex II Pro FPGA board which is used for PWM generation. A separate PC, also knows as a console, is connected to the simulator via eithernet so that a user can have access to the node through the communication between the host (console) and the target (node). Through the console the user is able to start and stop the experiment and to monitor

various signals being measured.

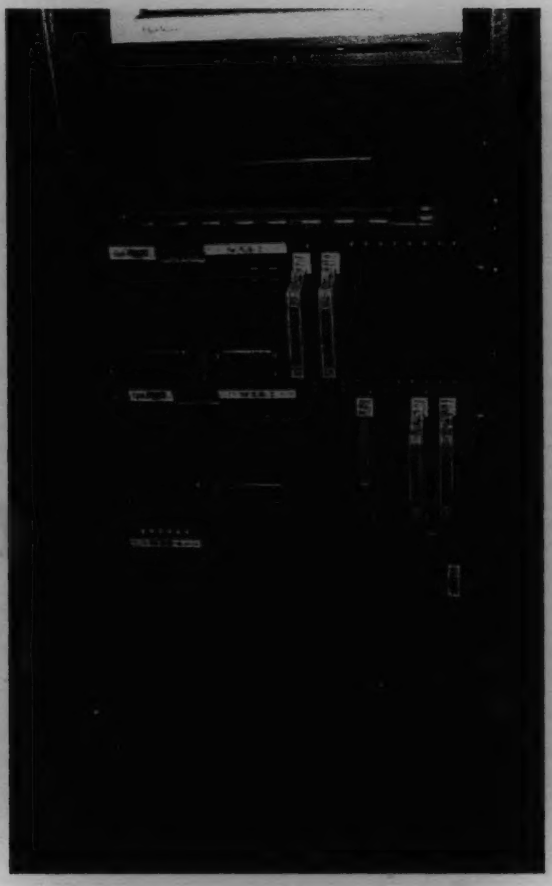


Figure 5.2: Real-time digital simulator

ADC and DAC

An analog-to-digital converter (ADC) has 16 channels and each channel performs a conversion of analog voltage into a 16 bit signal. The converted digital signal is interpreted as a signed 2's complement 16 bit fixed value with binary point at 10 (denoted Fix16_10) by the FPGA. Therefore the range of the analog input signal to the ADC is ± 16 V. Similarly, the digital-to-analog converter (DAC) takes the 16 bit signal (Fix16_10) and outputs an analog voltage within the range of ± 16 V. The conversion from digital to analog signal requires minimum of 2 μs.

Digital Output Card

The digital output card contains 16 channels of amplifiers which convert a 0 to 5 V digital output from the FPGA into 0 to 15 V digital signal. This amplification is necessary as the IGBTs in the VSC needs a minimum of 13 V in order to turn on. The digital output card is also equipped with opto-couplers which physically separate the digital simulator from the VSC to prevent damage in the case of high current flow into the digital output card.

FPGA board

The FPGA board which is installed inside one of the nodes in the digital simulator is used for generating sine PWM-based gating signals for the IGBTs. The Xilinx Virtex-II Pro has 11,088 logic cells and is based on a 100MHz IBM PowerPC processor. This leads to a 10 ns time step for the triangular carrier wave resolution. The FPGA receives the sinusoidal reference signals from the simulator, compares them with the internally generated 2 kHz triangular carrier wave, and sends the digital pulses to the VSC via the simulator's digital output card. Since the dead-time is already built in the gate drive board of the converter, dead-time implementation is not required on the FPGA circuit. Figure 5.3 shows the FPGA board which was custom designed by Opal-RT Technologies to be compatible with the simulator.

5.1.3 Summary of the Experimental Setup

In this section a complete hardware setup for the experiment is illustrated to show how each components are interconnected. Figure 5.4 is the complete diagram of the experimental setup. The real-time simulator can be split into four major parts in terms of their functionalities: the analog-to-digital converter, the processor, the FPGA board and the digital output card. The measured analog signals from the voltmeters and current sensors are first converted into digital signals. These signals are then used to compute the control algorithm which gives m_a and δ for PWM. These values are used to generate the 3-phase reference modulating signals $v_{mod,a}$, $v_{mod,b}$, and $v_{mod,c}$. These three signals are

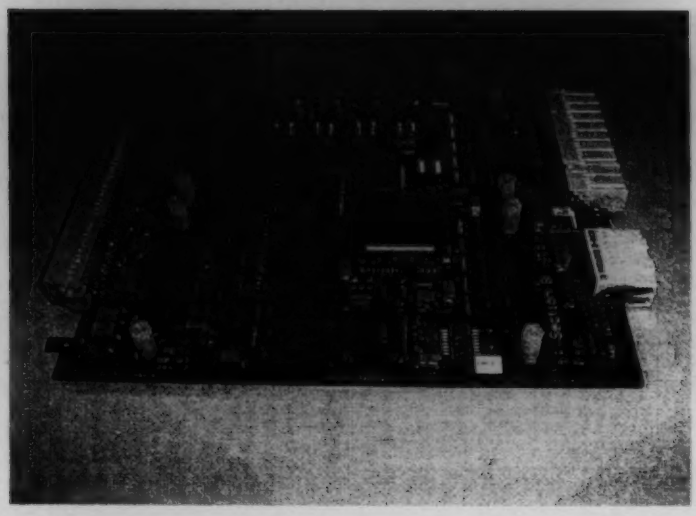


Figure 5.3: Xilinx Virtex-II Pro FPGA board

sent to the FPGA board so that the triangular carrier wave can be compared with the 3-phase modulating signals to generate PWM pulses. The generated gating pulses are then sent to the digital output card which amplifies the pulses and sends them to the gate drive board on the VSC.

The purpose of having the variac between the AC supply and the filter inductors is to be able to gradually charge the capacitor bank. This avoids the capacitors from instantly charging which can create large inrush current in the system. A 3-phase transformer is also added for safety reasons. A transformer physically separates the system from the 3-phase power supply to protect the system.

The control algorithm is implemented on MATLAB/Simulink using the RT-LAB toolbox provided by Opal-RT Technologies Inc. A complete block diagram of this implementation can be found in Appendix C (`pwm_tune.mdl`).

5.2 Reference Angle Generation

In order to generate the reference angle from the 3-phase supply, two differential voltage probes are connected between phase a and b, and between phase b and c (See Figure 5.4). From these two voltages, the reference angle can be

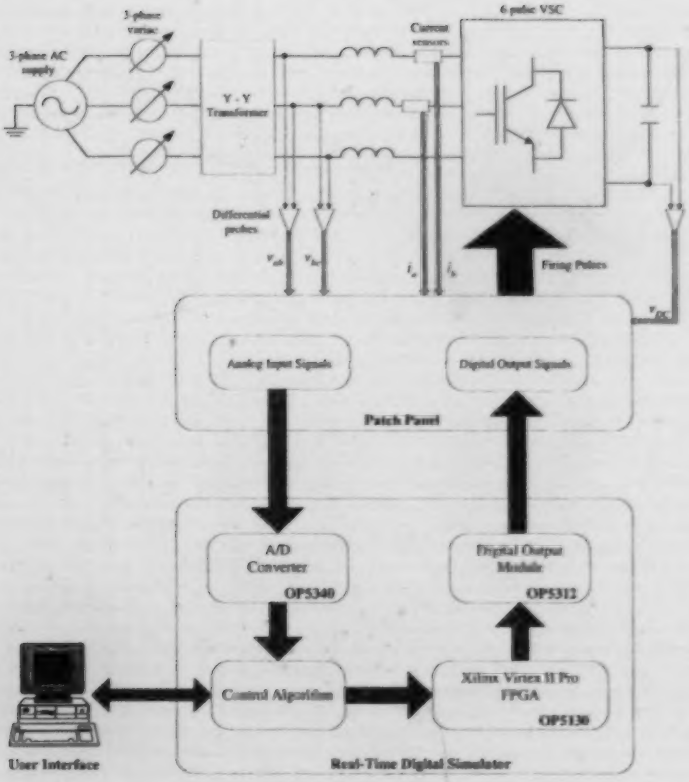


Figure 5.4: Experimental setup

computed. The expressions for v_a, v_b, and v_c are

$$\begin{aligned} v_a(t) &= \hat{V}\sin(\omega t) \\ v_b(t) &= \hat{V}\sin(\omega t - \frac{2\pi}{3}) \\ v_c(t) &= \hat{V}\sin(\omega t + \frac{2\pi}{3}). \end{aligned}$$

Hence,

$$\begin{aligned} v_{ab}(t) &= \hat{V}\sin(\omega t) - \hat{V}\left(\sin(\omega t)\cos(\frac{2\pi}{3}) - \cos(\omega t)\sin(\frac{2\pi}{3})\right) \\ &= \hat{V}\sin(\omega t) - \hat{V}\left(-\frac{1}{2}\sin(\omega t) - \frac{\sqrt{3}}{2}\cos(\omega t)\right) \\ &= \hat{V}\left(\frac{3}{2}\sin(\omega t) + \frac{\sqrt{3}}{2}\cos(\omega t)\right) \end{aligned}$$

and

$$v_{bc}(t) = \hat{V}\left(\sin(\omega t)\cos(\frac{2\pi}{3}) - \cos(\omega t)\sin(\frac{2\pi}{3})\right) - \hat{V}\left(\sin(\omega t)\cos(\frac{2\pi}{3}) + \cos(\omega t)\sin(\frac{2\pi}{3})\right)$$
$$= \hat{V}\left(-\frac{1}{2}\sin(\omega t) - \frac{\sqrt{3}}{2}\cos(\omega t) + \frac{1}{2}\sin(\omega t) - \frac{\sqrt{3}}{2}\cos(\omega t)\right)$$
$$= \hat{V}(-\sqrt{3}\cos(\omega t)).$$

This leads to

$$\hat{V}\sin(\omega t) = \frac{1}{3}(2v_{ab}(t) + v_{bc}(t))$$

and

$$\hat{V}\cos(\omega t) = -\frac{1}{\sqrt{3}}(v_{bc}(t)).$$

Hence, the reference angle is computed by

$$\omega t = \tan^{-1}\left(\frac{\sin(\omega t)}{\cos(\omega t)}\right) = \tan^{-1}\left(-\frac{\sqrt{3}(2v_{ab}(t) + v_{bc}(t))}{3v_{bc}(t)}\right).$$

5.3 PWM Implementation with an FPGA

PWM generation using FPGA technology has been performed in [6]. The hardware design of the FPGA consists of two main parts: a high frequency triangular carrier wave generation and pulse generation. Each component is explained in detail in the following subsections. The design is specifically implemented for the control sampling frequency of 4 kHz with a 2 kHz carrier frequency.

5.3.1 Triangular Carrier Wave Implementation

The triangular carrier wave with a period of 500 μs is generated internally in the FPGA using a 16 bit counter. Since the FPGA has a clock period of 10 ns, it is calculated that the counter should count up from -12500 to 12500 and then count down to -12500 in 500 μs. In order to synchronize the counter with the reference control signal, the digital simulator also needs to send a synchronizing signal which we call *sync* to the FPGA in addition to the 3 modulating signals. The *sync* signal is a pulse with 50 percent duty ratio with a frequency of 2 kHz.

The counter requires a reset port which resets the output of the counter to the initial value of -12500 (on the rising edges of the *sync* signal), a load port which loads either -12500 (for rising edges of *sync*) or 12500 (for falling edges of *sync*) at the output of the counter, and an up/down port (count up when *sync* is high and count down otherwise) which determines the direction of the counting. Although the modulating signals are bounded between -1 and 1 in the mathematical model, these signals are scaled by a factor of 12500 in order to match the carrier signal magnitude. Figure 5.5 shows the logic used to generate the carrier wave. The FPGA design is performed in MATLAB/Simulink using the Xilinx System Generator toolbox. A complete Simulink block diagram of the PWM implementation is included in Appendix D (`fpga_pwm.mdl`).

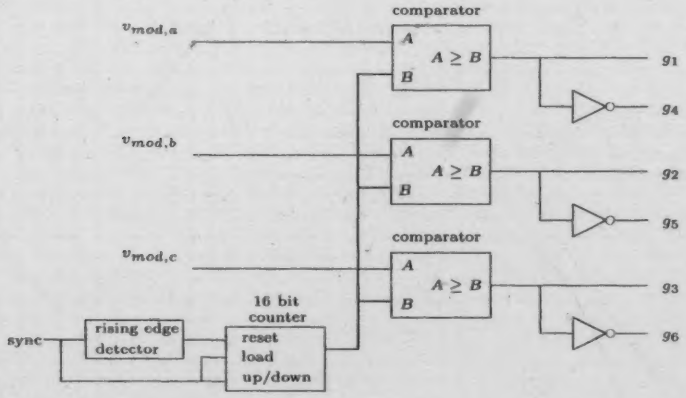


Figure 5.5: PWM generation in FPGA

5.3.2 Pulse Generation

The gate pulses for the three upper switches g_1, g_2, g_3 come from the output of the comparators in the FPGA and the lower gate signals g_4, g_5, g_6 are the inverted signals of their respective upper switches by a *not* gate. Since 2 μs of dead-time is already built in the gate drive board of the converter, dead-time implementation is not required on the FPGA. The Powerex inverter used in the experiment requires a minimum dead-time of 1.2 μs and to ensure that

switches have enough time to turn on and off, 2 μs of dead-time is appropriate.

Figure 5.6 shows typical sine PWM waveform of the upper switch of the VSC. Note that the time step of the sinusoidal modulating signal is 250 μs whereas the period of the carrier wave is 500 μs.

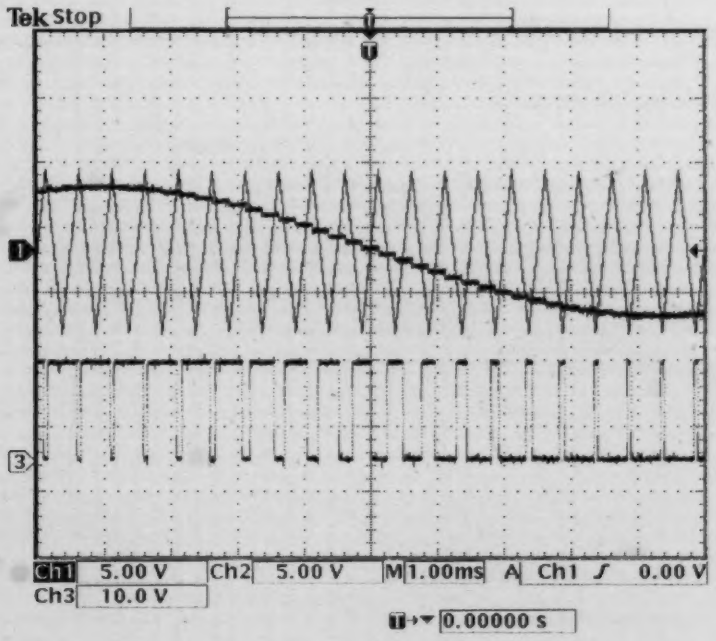


Figure 5.6: Typical sinusoidal PWM waveforms

5.4 Steady State Operation

In this section, we show the typical waveforms of the voltages and currents under steady state i.e., when the system is at equilibrium and is controlled in open-loop for fixed values of m_a and δ. Figure 5.7 shows a typical line-to-neutral voltage e_a at the AC terminal of the VSC. This image was captured with $m_a = 0.8$ and $\delta = 0$ with $v_{dc} = 200$ V. The figure demonstrates that sine PWM scheme is functioning as expected and that e_a is switching between 5 levels of voltages i.e., $\pm\frac{400}{3}$ V, $\pm\frac{200}{3}$ V, and 0 V. Figure 5.8 is the line-to-line voltage e_{ab} with the same m_a, δ, and v_{dc} where e_{ab} is switching between ± 200 V and 0 V. Figure 5.9 is the 3-phase currents i_a, i_b, i_c with inputs $m_a = 0.75$ and

$\delta = 4.5^o$.

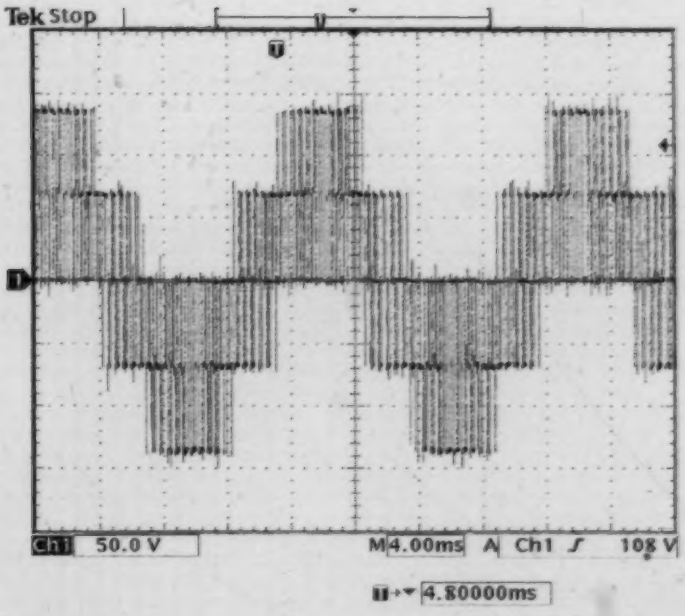


Figure 5.7: Typical waveform of the line-to-neutral AC terminal voltage

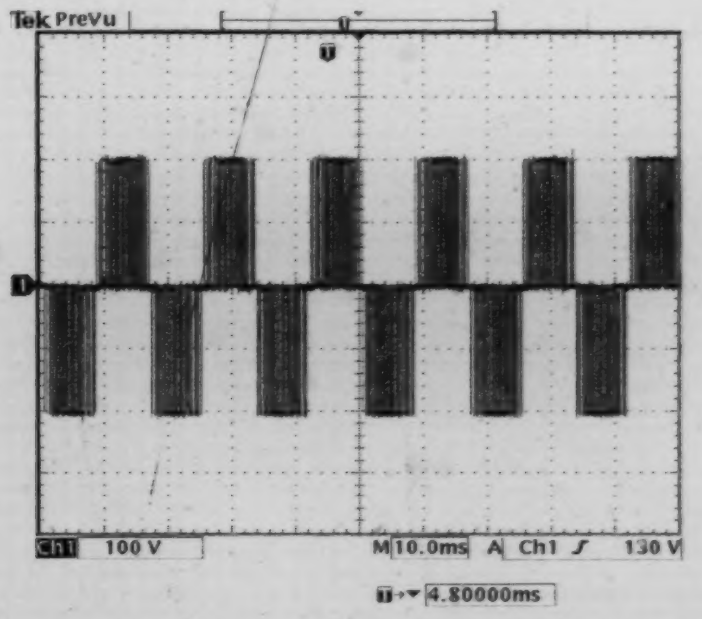


Figure 5.8: Typical waveform of the line-to-line AC terminal voltage

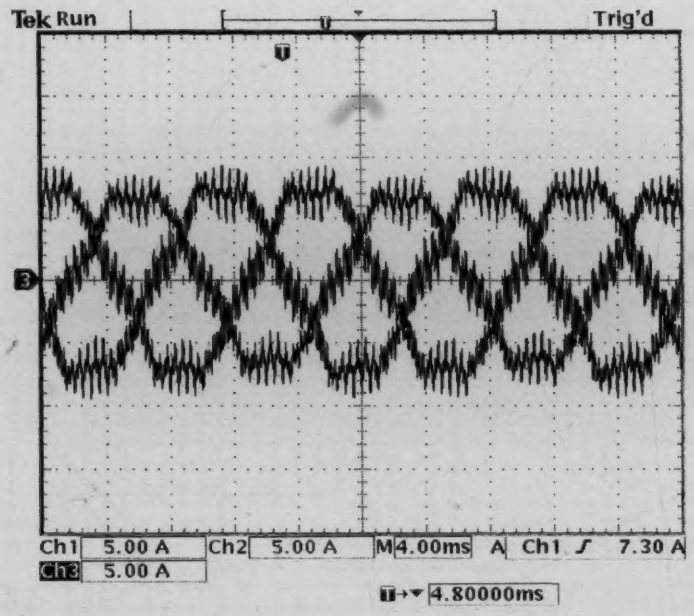


Figure 5.9: Typical waveform of the 3-phase AC currents

5.5 Filtering of Measurements

The AC voltages v_{ab}, v_{bc} and the DC voltage v_{dc} are measured using differential voltage probes and the 3-phase AC currents are measured using LEM Hall-Effect sensors. Due to the noise present in the measurements, the noise is filtered by taking the average over ten sampled data. Since the sampling frequency is 4 kHz i.e., the sampling period of 250 μs, this filtering causes a delay of $10 \cdot 250\ \mu s = 2.5\ ms$ since 10 samples have to be collected in order to take the average of the data.

5.6 Trajectory Tracking Control of i_q and v_{dc}

This section presents the results from the experimental setup of the flatness-based controlled PWM VSC. We make use of the open-loop trajectory described in Section 4.4.2 for driving the VSC system from $v_{dc} = 200$ V, $i_q = -10$ A to $v_{dc} = 240$ V, $i_q = 10$ A while respecting input constraints. Figure 5.10 shows the results of the tracking control of i_q and v_{dc} where the solid line is the measured signal and the dotted line is the reference. Due to the modeling error and disturbances, the trajectories do not exactly follow their references, but the closed-loop demonstrates good transient performance. These results were obtained with controller gains $k_1 = 1800\ \text{s}^{-3}$, $k_2 = 2600\ \text{s}^{-2}$, $k_3 = 100\ \text{s}^{-1}$, $k_4 = 2800\ \text{s}^{-2}$, $k_5 = 150\ \text{s}^{-1}$. The control signals are shown in Figure 5.11 with m_a and δ remaining within their allowed regions.

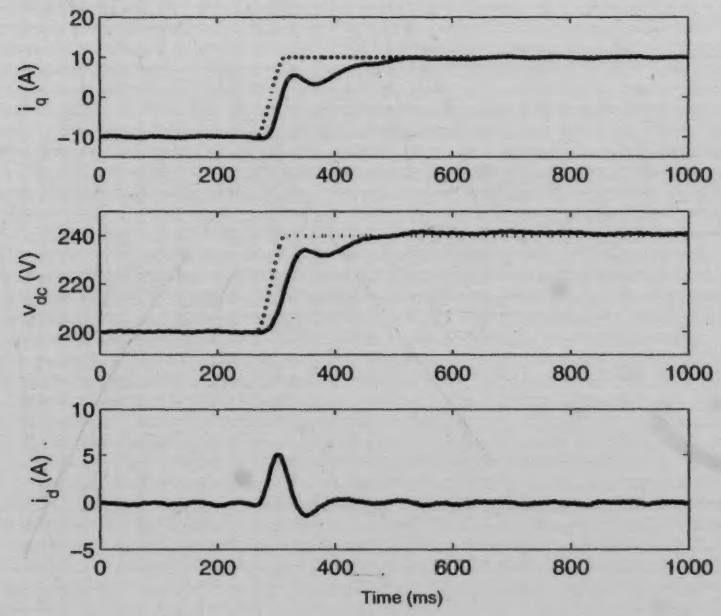


Figure 5.10: Experimental results of flatness-based control of i_q and v_{dc}

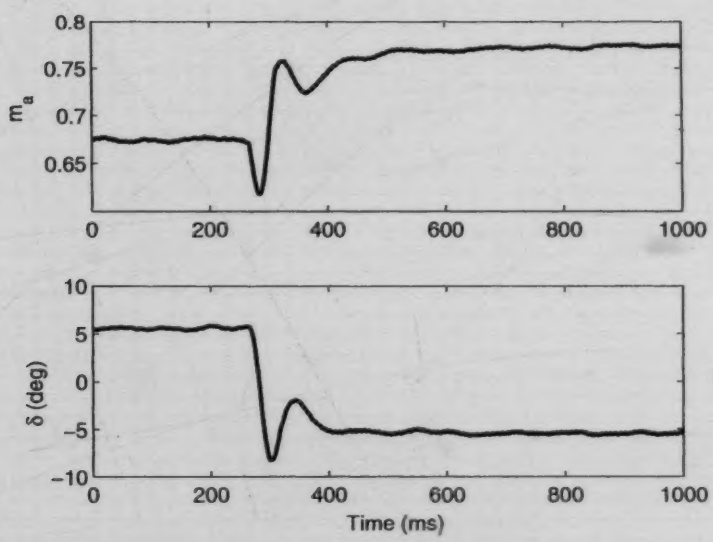


Figure 5.11: Flatness-based control inputs m_a and δ

5.7 Comparison with Vector Control

In this section we show the results for the system under the same setup as in the flatness-based control case except the decoupled vector control scheme is used to control the system. Figure 5.12 shows the results for a desired transition for i_q from -10 A to 10 A and v_{dc} from 200 V to 240 V where the solid line is the measured signal and the dotted line is the reference. Unlike in the nonlinear control, the reference inputs are discontinuous step functions. The corresponding control signal is shown in Figure 5.13. These results were obtained with controller gains $k_{id}^p = 3$ V/A, $k_{id}^i = 65$ V/(A$\cdot$ s), $k_{iq}^p = 3$ V/A, $k_{iq}^i = 65$ V/(A$\cdot$s), $k_v^p = 0.54$ A/V, $k_v^i = 10.8$ A/(V$\cdot$s) which were determined from an extensive tuning procedure [8], [27]. In terms of the settling time, both control methods provide a transition for i_q and v_{dc} of less than 200 ms. However, transient performance of the vector control is inferior to that of the nonlinear control in terms of high frequency oscillations in the controls and large overshoot in i_q and v_{dc}.

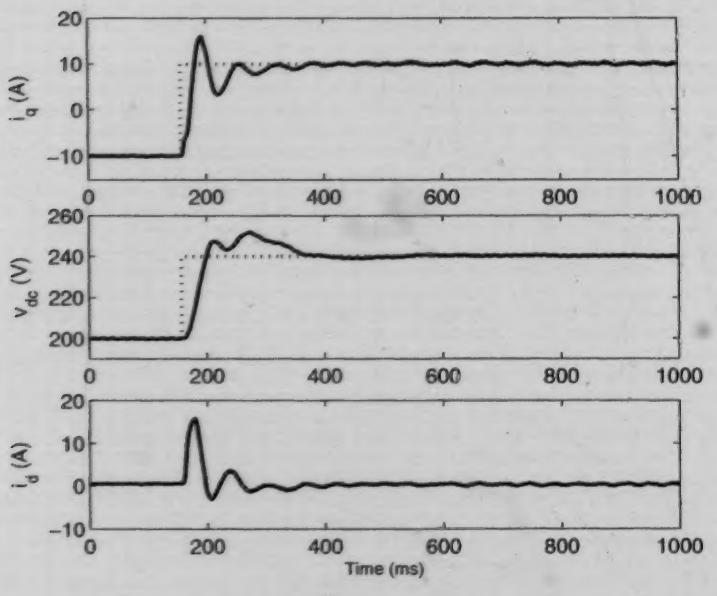


Figure 5.12: Step change in i_q and v_{dc} with vector control

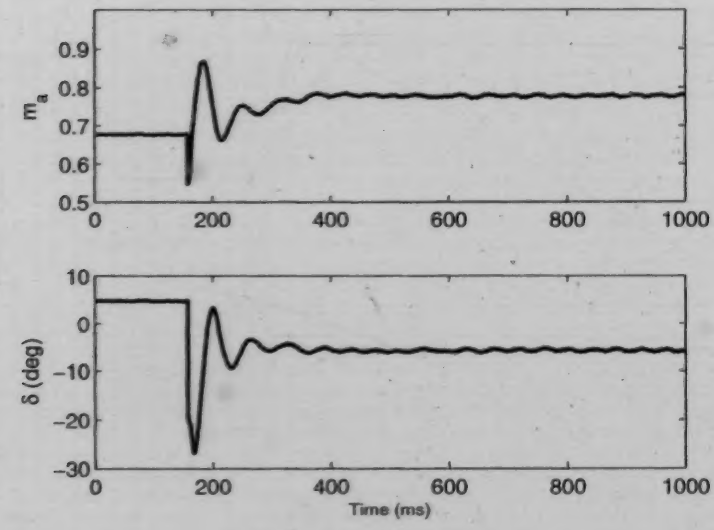


Figure 5.13: Control inputs m_a and δ for vector control

5.8 Summary

In this chapter we successfully implemented a flatness-based control on an actual VSC test stand. The hardware implementation of sine PWM and equipments used in the experiment are described in detail. Open-loop motion planning is used to steer the system between equilibria while respecting input and state constraints. Closed-loop control ensures that tracking is robust to model error, initial tracking condition error, and disturbances. Experimental results illustrate that the nonlinear control provides improved transient tracking performance relative to a traditional vector control method.

Chapter 6

Conclusion and Future Work

6.1 Summary of Research and Conclusion

In this thesis we considered the reactive current and DC voltage tracking control problem for a 3-phase PWM VSC for STATCOM applications. A VSC is the main building block of power flow controllers in Flexible AC Transmission Systems (FACTS) such as D-STATCOMs and UPFCs. This has led to the development of control algorithms for reactive current and DC voltage regulation and tracking control.

The conventional control technique for the VSC system is a decoupled vector control using PI compensators. This technique may be sufficient for industrial applications however, recent development in nonlinear control techniques has given the motivation for this thesis work which is focused on the investigation of advanced control algorithm for the VSC. The two main approach we took in nonlinear control design are feedback linearization and flatness-based motion planning control.

First we applied the feedback linearization technique to check whether the model is feedback linearizable. In Chapter 4 we have shown that the system under study is locally static state feedback linearizable and by the virtue of this property the system is necessarily flat. The flat outputs are chosen to be the lead components of the coordinate transformation, and open loop motion planning problem has been suggested. For relevant practical application, we have chosen the motion planning problem as the transition of i_q from -10 A to 10 A and v_{dc} from 200 V to 240 V in 50 ms. Due to the constraints in inputs

and in current ratings of the equipments, the motion planning problem also takes these constraints into consideration when designing the desired trajectory of the flat output. Closed-loop feedback control is incorporated into the controller to compensate for modeling error and disturbances.

Then we proceeded to the implementation and experimental verification of the flatness-based control approach to the actual VSC system. Sine PWM implementation is done on the FPGA device as this approach is commonly used in industry. Two control techniques are implemented on the same test stand: flatness-based control and the traditional decoupled vector control. The results for both control algorithm are plotted and are compared. The results show the improved transient response of both i_q and v_{dc} in terms of settling time and over shoot. This demonstrates that flatness-based control technique works in practice and out performs the conventional vector control scheme in reference transitions of currents and DC voltages.

6.2 Future Work

Presently, the proposed control performs open-loop motion planning off-line. This can be a major drawback of flatness-based open-loop control technique. A natural extension to the work in this thesis would be an on-line trajectory planning of the flat output if possible. Another approach to this problem is to construct a look-up table for the reference trajectories of the flat outputs in order to streamline the implementation. Other areas where this work can be extended to are: the exact modeling of the VSC system including switching harmonics, the VSC control system for the unbalanced 3-phase AC supply, flat output parametrization using basis functions other than polynomials such as b-spline basis functions.

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Appendix A

Differential Geometry

Basic definitions of differential geometry is reviewed in this appendix since the majority of the discussions in Chapter 4 assume a basic knowledge of this theory. Feedback linearization technique makes use of the notion of differential geometry and here we briefly review several definitions. For a complete introduction to differential geometry see the text by [16]. The content of this appendix can also be found in [21].

Diffeomorphisms

Let p be a point in E^n, an $n-$dimensional Euclidean space, and U, a neighborhood of p. Let $\varphi(p) = (x_1(p), \cdots, x_n(p)) : U \to V \subset \mathbb{R}^n$ be a homeomorphism i.e., one-to-one and onto (a bijection), with φ and φ^{-1} continuous. A set (U, φ) is called a *coordinate neighborhood* or a *coordinate chart*. If both φ and φ^{-1} are smooth maps in V, then φ is called a *local diffeomorphism*. If both φ and φ^{-1} are smooth maps in $\mathbb{R}^n$, then φ is called a *global diffeomorphism*.

Vector Fields

A *vector field* f on an open subset $U \subset \mathbb{R}^n$ is a function which assigns to each point $p \in U$ a vector f_p. For a coordinate chart (U, φ), if $x_1(p), \cdots, x_n(p), p \in U$ are local coordinates, a C^∞ (smooth) vector field f is expressed as

$$f = f_1(x)\frac{\partial}{\partial x_1} + \cdots + f_n(x)\frac{\partial}{\partial x_n}$$

with $f_i \in C^\infty(p)$. A vector field may also be expressed as a column vector as

$$f(x) = \begin{bmatrix} f_1(x) \\ \vdots \\ f_n(x) \end{bmatrix}.$$

Lie Derivatives

If f is a smooth vector field on U and h is a smooth function where $h : U \subset \mathbb{R}^n \to \mathbb{R}$, then $f(h)$ is a smooth function on U defined by

$$f(h)(p) = \sum_{i=1}^{n} f_i(p) \left(\frac{\partial h}{\partial x_i} \right)(p).$$

The function $f(h)$ is called the *Lie Derivative* of the function h along the vector field f. Lie derivatives are often denoted as $L_f h$ which can conveniently denote repeated operations. For example, taking the Lie derivative i times along the same vector field f can be denoted

$$L_f^i h = L_f(L_f^{i-1} h)$$

with

$$L_f^1 h = L_f h, \quad L_f^0 h = h.$$

The *Lie Bracket* of two vector fields f, g is defined by

$$[f, g](h) = f(g(h)) - g(f(h)) = L_f L_g h - L_g L_f h$$

We remark that the Lie bracket $[f, g]$ is also a vector field [21]. The Lie bracket $[f, g]$ is also denoted by $\mathrm{ad}_f g$ which can simplify the notation for iterated Lie brackets as

$$\mathrm{ad}_f^i g = ad_f(\mathrm{ad}_f^{i-1} g), \ \mathrm{ad}_f^1 g = ad_f g, \ \mathrm{ad}_f^0 g = g.$$

If we define f and g in local coordinates $(x_1, \cdots, x_n)$ as

$$f = \sum_{i=1}^{n} f_i \frac{\partial}{\partial x_i}, \quad g = \sum_{j=1}^{n} g_j \frac{\partial}{\partial x_j}$$

then $ad_f g$ can be written in vector notation as

$$ad_f g = \frac{dg}{dx} f - \frac{df}{dx} g,$$

where

$$\frac{df}{dx} = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \cdots & \frac{\partial f_1}{\partial x_n} \\ \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial x_1} & \cdots & \frac{\partial f_n}{\partial x_n} \end{bmatrix}.$$

Distributions

An r-dimensional *distribution* $\mathcal{D}$ on W, an open connected subset of $\mathbb{R}^n$, is a map which assigns to each point $p \in W$ an r-dimensional subspace of $\mathbb{R}^n$ such that for each $p_o \in W$ there exists a neighborhood U of p_o and r smooth vector fields $f_1, \cdots, f_r$ with the following properties:

1. $f_1(p), \cdots, f_r(p)$ are linearly independent for every $p \in U$,
2. $\mathcal{D}(p) = \text{span}\{f_1(p), \ldots, f_r(p)\}, \ \forall p \in U$.

A distribution $\mathcal{D}$ is said to be *involutive* if, given any two vector fields f and g belonging to $\mathcal{D}$, their Lie bracket $[f, g]$ also belongs to $\mathcal{D}$.

Appendix B

Simulation Program

The MATLAB file fseminf_flat.m solves the optimization problem over a semi-infinite constraints.

B.1 fseminf_flat.m

```
% Initial condition
x0 =[-0.2273 0.7396 1.1664 -0.0029 0.0355 -0.2418 0.7098];
% set maximum number of iteration and function evaluation
options =optimset('MaxFunEvals',10000,'MaxIter',500);
[x,fval,exitflag,output]=
fseminf(@myfun, x0, 6, @constraints,[],[],[],[],[],[],options)
```

B.2 constraints.m

```
function [c,ceq,K1,K2,K3,K4,K5,K6,s]=constraints(x,s)

global L C Rc Rs w k vd t0 t1 vdc0 vdc1 iq0 iq1 dt A1 A2

if isnan(s(1,1)),
s = [dt/1000 0;dt/1000 0;dt/1000 0;dt/1000 0;dt/1000 0;dt/1000 0];
end
```

```
% Sample set
ta = t0:s(1,1):t1;
tb = t0:s(2,1):t1;
tc = t0:s(3,1):t1;
td = t0:s(4,1):t1;
te = t0:s(5,1):t1;
tf = t0:s(6,1):t1;

% expressions for a1, a2, a3, ...
% Note that y1 has 6 constraints and y2 has 4 constraints.

a16 = 1e10*x(1);
a17 = 1e10*x(2);
a18 = 1e10*x(3);

a24 = 1e10*x(4);
a25 = 1e10*x(5);
a26 = 1e10*x(6);
a27 = 1e10*x(7);

a10 = (3*L*power(iq0,2) + 2*C*power(vdc0,2))/4;
a11 = 0;
a12 = 0;
a13 = -(power(dt,-3)*(50400*(3*(iq0 - iq1)*(iq0 + iq1)*L +
2*C*(vdc0 - vdc1)*(vdc0 + vdc1)) +
(28*a16 + 3*dt*(4*a17 + a18*dt))*power(dt,6)))/3360;
a14 = (power(dt,-4)*(151200*(3*(iq0 - iq1)*(iq0 + iq1)*L +
2*C*(vdc0-vdc1)*(vdc0+vdc1))+168*a16*power(dt,6)
+(64*a17+15*a18*dt)*power(dt,7)))/1680;
a15 = -(power(dt,-5)*(30240*(3*(iq0 - iq1)*(iq0 + iq1)*L +
2*C*(vdc0-vdc1)*(vdc0+vdc1))+84*a16*power(dt,6)
+(24*a17+5*a18*dt)*power(dt,7)))/168;
```

```
a20 = iq0;
a21 = 0;
a22 = -(power(dt,-2)*(15120*iq0 - 15120*iq1 - 210*a24*
power(dt,4)- 84*a25*power(dt,5) - 21*a26*power(dt,6)
-4*a27*power(dt,7)))/2520;
a23 = -(power(dt,-3)*(-10080*iq0 + 10080*iq1 +420*a24*
power(dt,4)+ 126*a25*power(dt,5) + 28*a26*power(dt,6) +
5*a27*power(dt,7)))/840;

A1 = [a10, a11, a12, a13, a14, a15, a16, a17, a18];
A2 = [a20, a21, a22, a23, a24, a25, a26, a27];

% expressions for y, ydot, yddot from mathematica, y has N-4 coeff.
% evaluate y(t,x), ydot(t,x), yddot(t,x)

y1a = a10 + a11.*(ta-t0) + a12/Factorial(2).*(ta-t0).^2 +
a13/Factorial(3).*(ta-t0).^3 + a14/Factorial(4).*(ta-t0).^4 +
a15/Factorial(5).*(ta-t0).^5 + a16/Factorial(6).*(ta-t0).^6 +
a17/Factorial(7).*(ta-t0).^7 + a18/Factorial(8).*(ta-t0).^8;

y1b = a10 + a11.*(tb-t0) + a12/Factorial(2).*(tb-t0).^2 +
a13/Factorial(3).*(tb-t0).^3 + a14/Factorial(4).*(tb-t0).^4 +
a15/Factorial(5).*(tb-t0).^5 + a16/Factorial(6).*(tb-t0).^6 +
a17/Factorial(7).*(tb-t0).^7 + a18/Factorial(8).*(tb-t0).^8;

y1c = a10 + a11.*(tc-t0) + a12/Factorial(2).*(tc-t0).^2 +
a13/Factorial(3).*(tc-t0).^3 + a14/Factorial(4).*(tc-t0).^4 +
a15/Factorial(5).*(tc-t0).^5 + a16/Factorial(6).*(tc-t0).^6 +
a17/Factorial(7).*(tc-t0).^7 + a18/Factorial(8).*(tc-t0).^8;

y1d = a10 + a11.*(td-t0) + a12/Factorial(2).*(td-t0).^2 +
```

```
a13/Factorial(3).*(td-t0).^3 + a14/Factorial(4).*(td-t0).^4 +
a15/Factorial(5).*(td-t0).^5 + a16/Factorial(6).*(td-t0).^6 +
a17/Factorial(7).*(td-t0).^7 + a18/Factorial(8).*(td-t0).^8;

y1a_dot = a11 + a12*(-t0 + ta) + (a13*power(-t0 + ta,2))/2.  +
(a14*power(-t0 + ta,3))/6.  + (a15*power(-t0 + ta,4))/24.  +
(a16*power(-t0 + ta,5))/120.  + (a17*power(-t0 + ta,6))/720.  +
(a18*power(-t0 + ta,7))/5040;

y1b_dot = a11 + a12*(-t0 + tb) +
(a13*power(-t0 + tb,2))/2.  + (a14*power(-t0 + tb,3))/6.  +
(a15*power(-t0 + tb,4))/24.  + (a16*power(-t0 + tb,5))/120.  +
(a17*power(-t0 + tb,6))/720.  + (a18*power(-t0 + tb,7))/5040;

y1c_dot = a11 + a12*(-t0 + tc) + (a13*power(-t0 + tc,2))/2.  +
(a14*power(-t0 + tc,3))/6.  + (a15*power(-t0 + tc,4))/24.  +
(a16*power(-t0 + tc,5))/120.  + (a17*power(-t0 + tc,6))/720.  +
(a18*power(-t0 + tc,7))/5040;

y1d_dot = a11 + a12*(-t0 + td) +
(a13*power(-t0 + td,2))/2.  + (a14*power(-t0 + td,3))/6.  +
(a15*power(-t0 + td,4))/24.  + (a16*power(-t0 + td,5))/120.  +
(a17*power(-t0 + td,6))/720.  + (a18*power(-t0 + td,7))/5040;

y1a_ddot = a12 + a13*(-t0 + ta) + (a14*power(-t0 + ta,2))/2.  +
(a15*power(-t0 + ta,3))/6.  + (a16*power(-t0 + ta,4))/24.  +
(a17*power(-t0 + ta,5))/120.  + (a18*power(-t0 + ta,6))/720;

y1b_ddot = a12 + a13*(-t0 + tb) + (a14*power(-t0 + tb,2))/2.  +
(a15*power(-t0 + tb,3))/6.  + (a16*power(-t0 + tb,4))/24.  +
(a17*power(-t0 + tb,5))/120.  + (a18*power(-t0 + tb,6))/720;
```

```
y1c_ddot = a12 + a13*(-t0 + tc) + (a14*power(-t0 + tc,2))/2.  +
(a15*power(-t0 + tc,3))/6.  + (a16*power(-t0 + tc,4))/24.  +
(a17*power(-t0 + tc,5))/120.  + (a18*power(-t0 + tc,6))/720;

y1d_ddot = a12 + a13*(-t0 + td) + (a14*power(-t0 + td,2))/2.  +
(a15*power(-t0 + td,3))/6.  + (a16*power(-t0 + td,4))/24.  +
(a17*power(-t0 + td,5))/120.  + (a18*power(-t0 + td,6))/720;

y2a = a20 + a21*(-t0 + ta) + (a22*power(-t0 + ta,2))/2.  +
(a23*power(-t0 + ta,3))/6.  + (a24*power(-t0 + ta,4))/24.  +
(a25*power(-t0 + ta,5))/120.  + (a26*power(-t0 + ta,6))/720.  +
(a27*power(-t0 + ta,7))/5040;

y2b = a20 + a21*(-t0 + tb) + (a22*power(-t0 + tb,2))/2.  +
(a23*power(-t0 + tb,3))/6.  + (a24*power(-t0 + tb,4))/24.  +
(a25*power(-t0 + tb,5))/120.  + (a26*power(-t0 + tb,6))/720.  +
(a27*power(-t0 + tb,7))/5040;

y2c = a20 + a21*(-t0 + tc) + (a22*power(-t0 + tc,2))/2.  +
(a23*power(-t0 + tc,3))/6.  + (a24*power(-t0 + tc,4))/24.  +
(a25*power(-t0 + tc,5))/120.  + (a26*power(-t0 + tc,6))/720.  +
(a27*power(-t0 + tc,7))/5040;

y2d = a20 + a21*(-t0 + td) +
(a22*power(-t0 + td,2))/2.  + (a23*power(-t0 + td,3))/6.  +
(a24*power(-t0 + td,4))/24.  + (a25*power(-t0 + td,5))/120.  +
(a26*power(-t0 + td,6))/720.  + (a27*power(-t0 + td,7))/5040;

y2e = a20 + a21*(-t0 + te) + (a22*power(-t0 + te,2))/2.  +
(a23*power(-t0 + te,3))/6.  + (a24*power(-t0 + te,4))/24.  +
(a25*power(-t0 + te,5))/120.  + (a26*power(-t0 + te,6))/720.  +
(a27*power(-t0 + te,7))/5040;
```

```
y2f = a20 + a21*(-t0 + tf) + (a22*power(-t0 + tf,2))/2.  +
(a23*power(-t0 + tf,3))/6.  + (a24*power(-t0 + tf,4))/24.  +
(a25*power(-t0 + tf,5))/120.  + (a26*power(-t0 + tf,6))/720.  +
(a27*power(-t0 + tf,7))/5040;

y2a_dot = a21 + a22*(-t0 + ta) + (a23*power(-t0 + ta,2))/2.  +
(a24*power(-t0 + ta,3))/6.  + (a25*power(-t0 + ta,4))/24.  +
(a26*power(-t0 + ta,5))/120.  + (a27*power(-t0 + ta,6))/720;

y2b_dot = a21 + a22*(-t0 + tb) + (a23*power(-t0 + tb,2))/2.  +
(a24*power(-t0 + tb,3))/6.  + (a25*power(-t0 + tb,4))/24.  +
(a26*power(-t0 + tb,5))/120.  + (a27*power(-t0 + tb,6))/720;

y2c_dot = a21 + a22*(-t0 + tc) + (a23*power(-t0 + tc,2))/2.  +
(a24*power(-t0 + tc,3))/6.  + (a25*power(-t0 + tc,4))/24.  +
(a26*power(-t0 + tc,5))/120.  + (a27*power(-t0 + tc,6))/720;

y2d_dot = a21 + a22*(-t0 + td) + (a23*power(-t0 + td,2))/2.  +
(a24*power(-t0 + td,3))/6.  + (a25*power(-t0 + td,4))/24.  +
(a26*power(-t0 + td,5))/120.  + (a27*power(-t0 + td,6))/720;

% evaluate expr for u (y,ydot,yddot)
x1a = 2*y1a_dot/3/vd; %for plotting

arga = 2/C*y1a -2*L*(y1a_dot.^2)/3/C/(vd^2) -3*L/2/C.*(y2a.^2);
argb = 2/C*y1b -2*L*(y1b_dot.^2)/3/C/(vd^2) -3*L/2/C.*(y2b.^2);
argc = 2/C*y1c -2*L*(y1c_dot.^2)/3/C/(vd^2) -3*L/2/C.*(y2c.^2);
argd = 2/C*y1d -2*L*(y1d_dot.^2)/3/C/(vd^2) -3*L/2/C.*(y2d.^2);

x_3a = sqrt(arga);
x_3b = sqrt(argb);
```

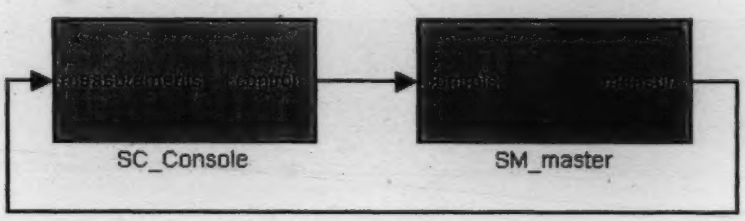
```
x_3c = sqrt(argc);
x_3d = sqrt(argd);

x1a_real = (-3*C*Rc*vd + sqrt(9*power(C,2)*power(Rc,2)*power(vd,2)+
12*(L - C*Rc*Rs)*(4*y1a + 2*C*Rc*y1a_dot - 3*(L -
C*Rc*Rs)*power(y2a,2))))/(6.*(L - C*Rc*Rs));

x3a_real = sqrt((Rc*(C*Rc*(-3*L*power(vd,2) + 8*power(Rs,2)*y1a +
4*L*Rs*y1a_dot) + L*(-8*Rs*y1a - 4*L*y1a_dot +
vd*sqrt(9*power(C,2)*power(Rc,2)*power(vd,2) +
12*(L - C*Rc*Rs)*(4*y1a + 2*C*Rc*y1a_dot -
3*(L - C*Rc*Rs)*power(y2a,2))))))/power(L - C*Rc*Rs,2))/2;

x1c_real = (-3*C*Rc*vd + sqrt(9*power(C,2)*power(Rc,2)*power(vd,2)+
12*(L - C*Rc*Rs)*(4*y1c + 2*C*Rc*y1c_dot -
3*(L - C*Rc*Rs)*power(y2c,2))))/(6.*(L - C*Rc*Rs));

x3c_real = sqrt((Rc*(C*Rc*(-3*L*power(vd,2) + 8*power(Rs,2)*y1c +
4*L*Rs*y1c_dot) + L*(-8*Rs*y1c - 4*L*y1c_dot + vd*sqrt(9*power(C,2)*
power(Rc,2)*power(vd,2) + 12*(L - C*Rc*Rs)*(4*y1c + 2*C*Rc*y1c_dot
- 3*(L - C*Rc*Rs)*power(y2c,2))))))/power(L - C*Rc*Rs,2))/2;

u1a = (-4*L/3/vd*y1a_ddot + 2*(vd+w*L*y2a))./x_3a;
u2c = -(2*L*y2c_dot + 4*w*L/3/vd*y1c_dot)./x_3c;

u1a_real = -(-2.*(6.*L.*Rc.*y2a.*(L.*w.*x1a_real + Rs.*y2a) +
4.*L.*power(x3a_real,2) + C.*power(Rc,2).*(3.*(vd -
2.*Rs.*x1a_real).*(vd - Rs.*x1a_real + L.*w.*y2a) -
2.*L.*y1a_ddot)) - 12.*L.*Rc.*(L-C.*Rc.*Rs).*y2a.*y2a_dot)./
(3.*Rc.*(2.*L.*x1a_real + C.*Rc.*(vd -2.*Rs.*x1a_real)).*
x3a_real);
```

```
u2c_real = (-2.*(Rs.*y2c + L.*(w.*x1c_real + y2c_dot))).\x3c_real;

K1 = (4*L/3/vd*y1a_ddot - 2*(vd+w*L*y2a))+0.01;
K2 = ((-4*L/3/vd*y1b_ddot + 2*(vd+w*L*y2b))).^2 - argb;
K3 = (2*L*y2c_dot + 4*w*L/3/vd*y1c_dot).^2 - argc;
K4 = -argd;
K5 = y2e-30;
K6 = -y2f-30;

c = []; ceq = [];

% Plot a graph of semi-infinite constraints
figure(1)
subplot(321)
plot(ta,u1a,'-',tc,u2c,'-.');
title('u1 and u2')
subplot(322)
plot(ta,x_3a,'-',ta,y2a,':');
title('trajectories of v_dc and i_q')
subplot(323)
plot(ta,x3a_real,'-',ta,x_3a,':');
title('x3_real and x3')
subplot(324)
plot(ta,x1a_real,'-',ta,x1a,':');
title('x1_real and x1')
subplot(325)
plot(ta,u1a_real,'-',ta,u1a,':');
title('u1_real and u1')
subplot(326)
plot(tc,u2c_real,'-',tc,u2c,':');
title('u2_real and u2')
drawnow
```

Appendix C

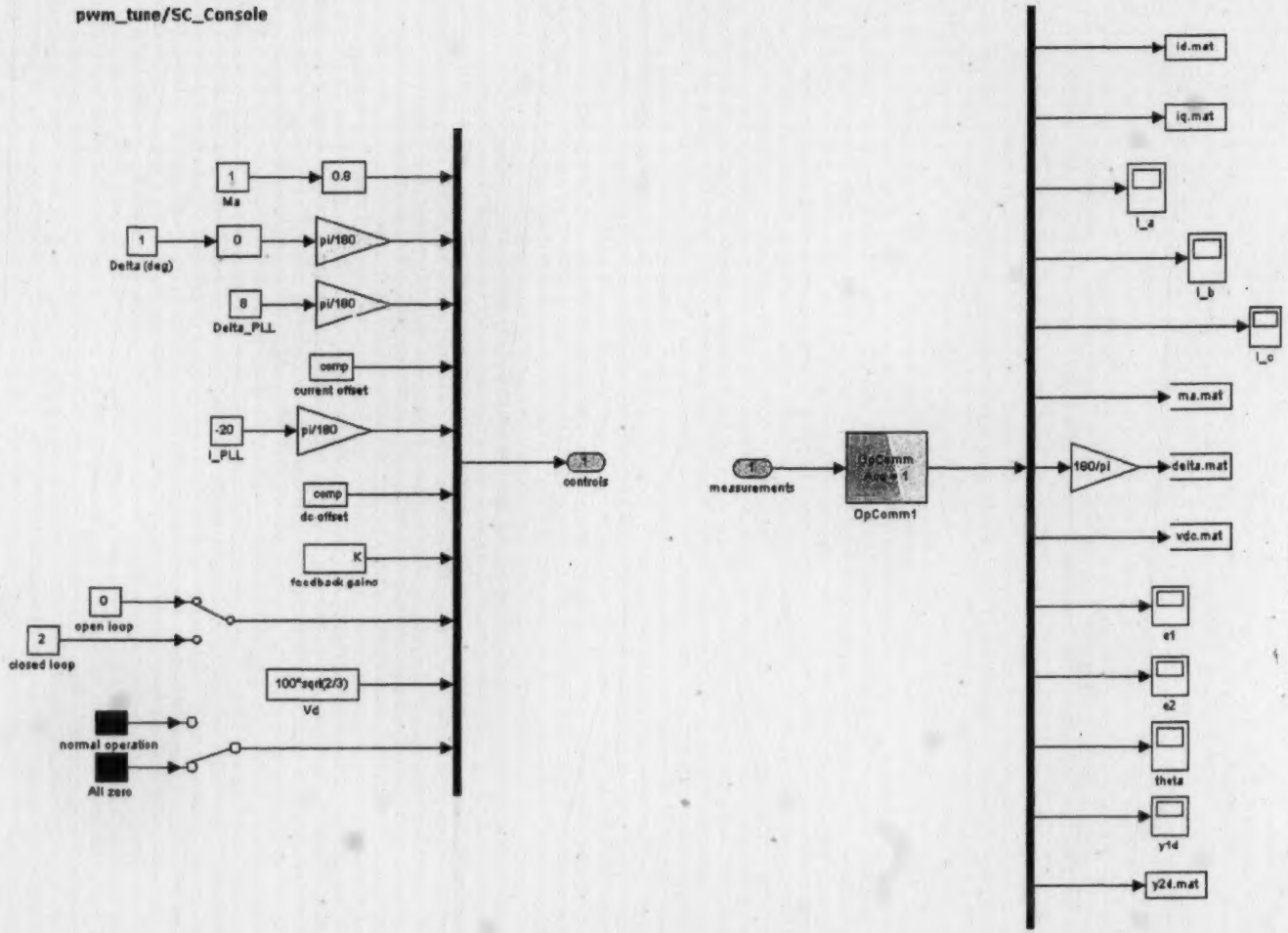
RT-LAB Model

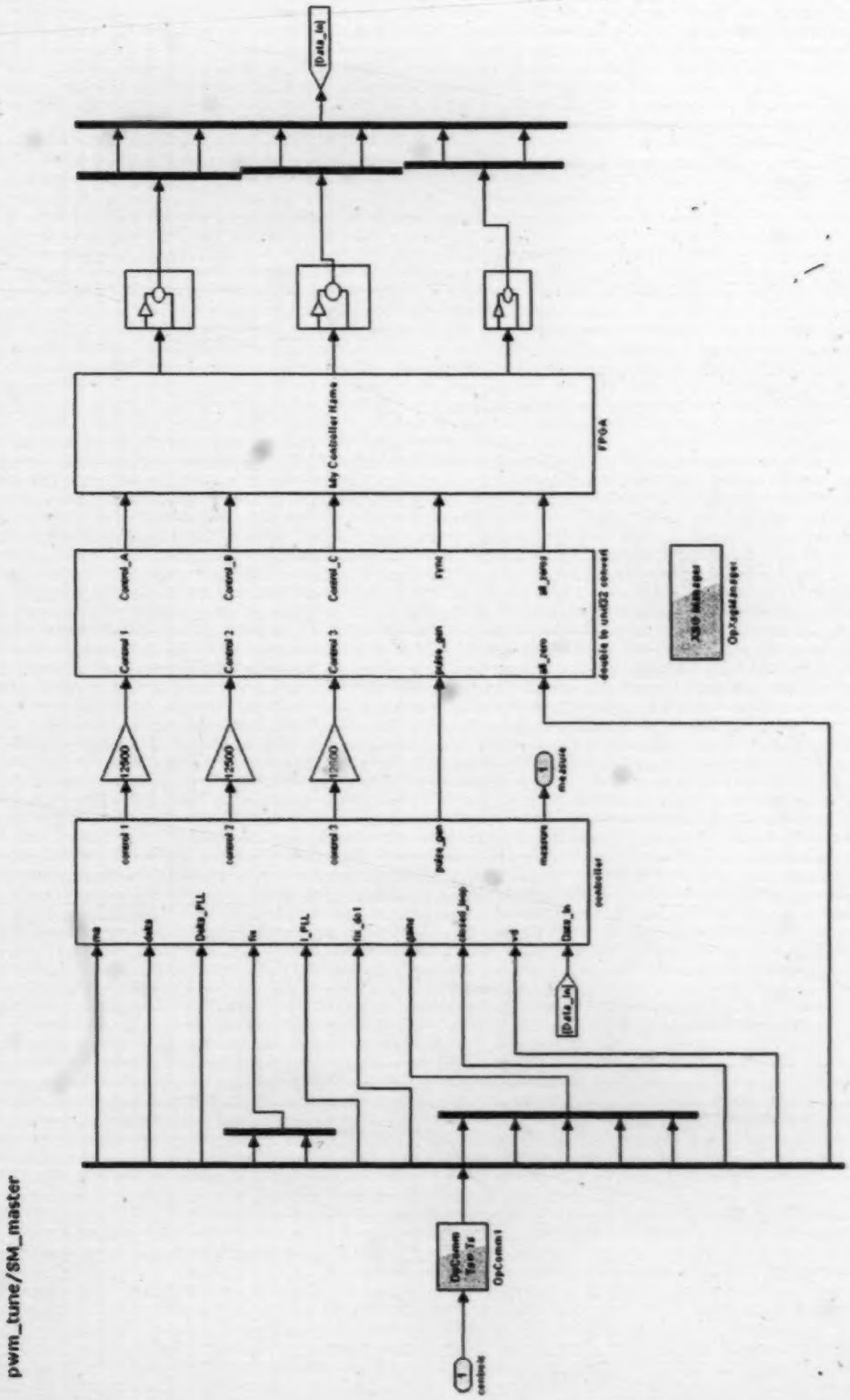
pwm_tune.mdl

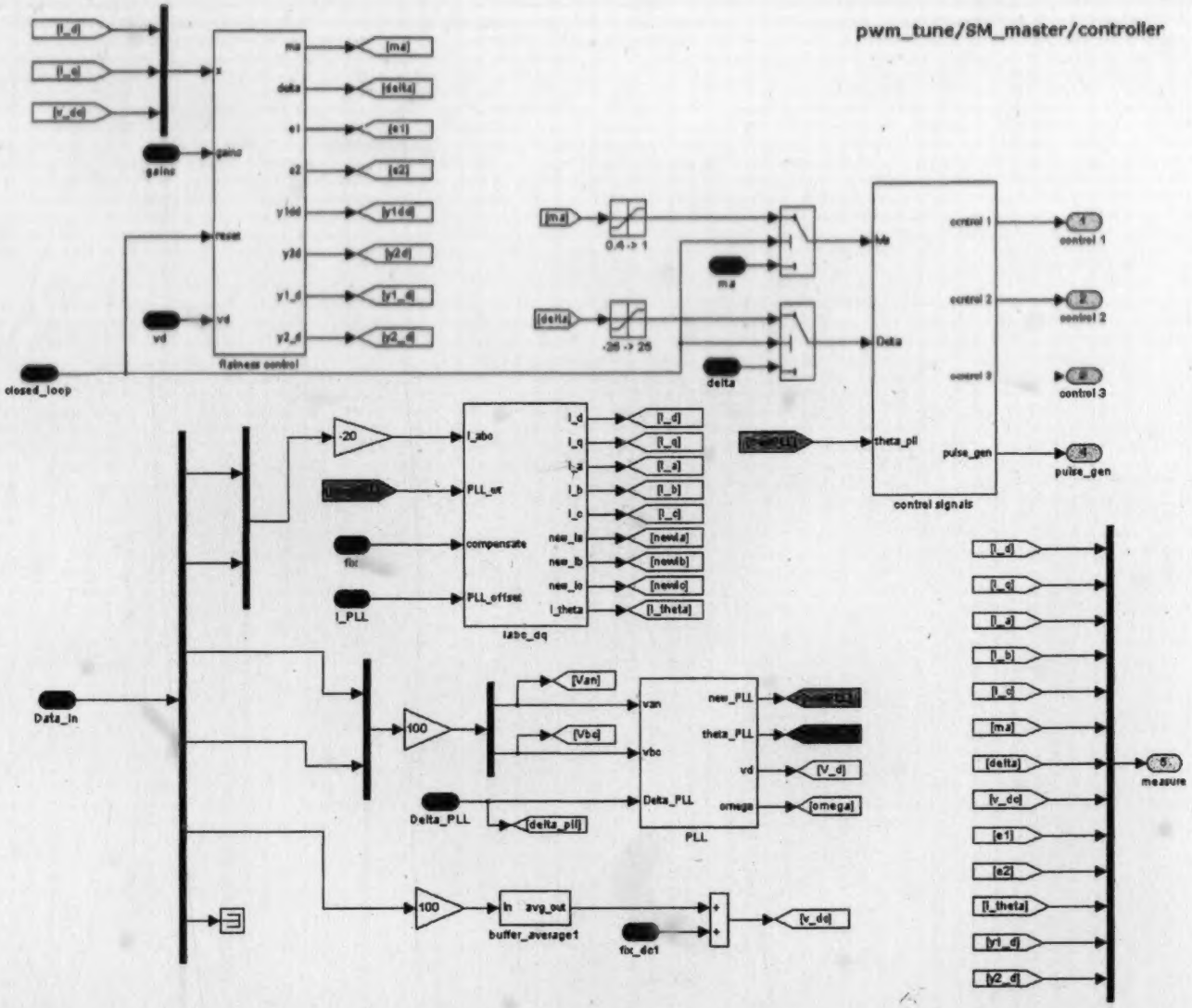


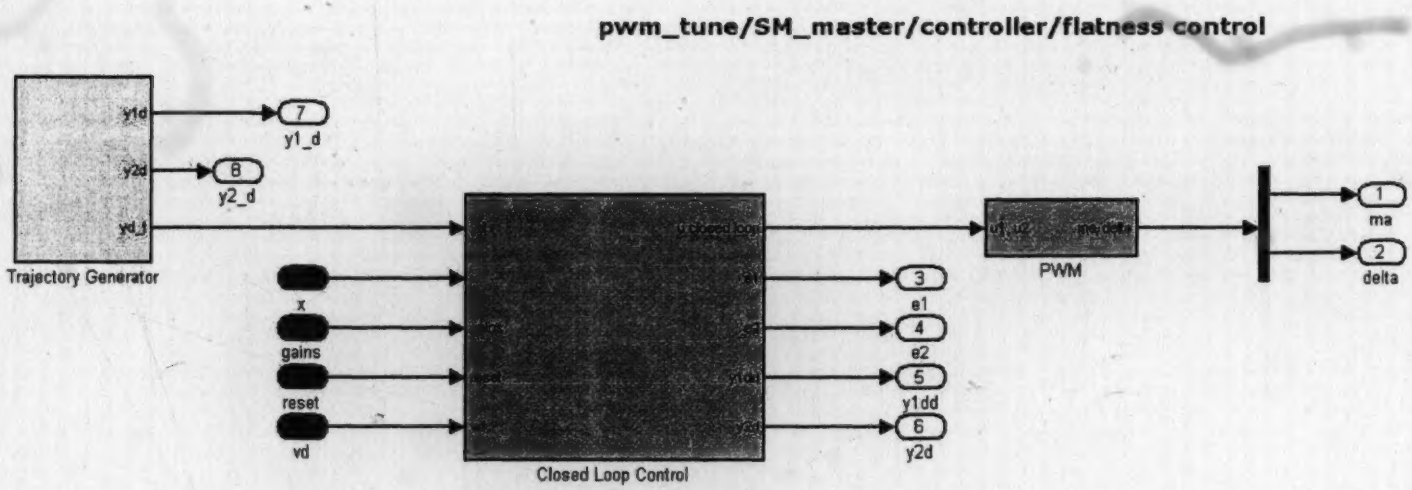
Flatness-based control model for RT-LAB 8.0.2

Ts = 250e-6,

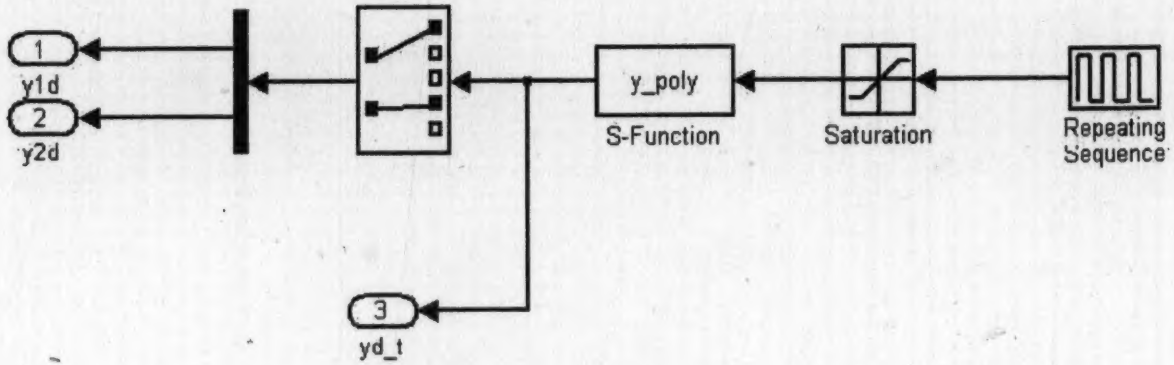

pwm_tune/SC_Console
1
Ma
0.8
1
Delta (deg)
0
pi/180
8
Delta_PLL
pi/180
comp
current offset
-20
I_PLL
pi/180
comp
dc offset
K
feedback gain
0
open loop
2
closed loop
100*sqrt(2/3)
Vd
normal operation
All zero
controls
1
measurements
OpComm
OpComm1
id.mat
iq.mat
I_a
I_b
I_c
ma.mat
180/pi
delta.mat
vdc.mat
e1
e2
theta
y1d
y24.mat


pwm_tune/SM_master
FPGA
My Controller Name
double to uint32 convert
X86 Manager
OpCommand
OpCommand Type 7a
12500
12500
12500
Data_FLL
Data_in

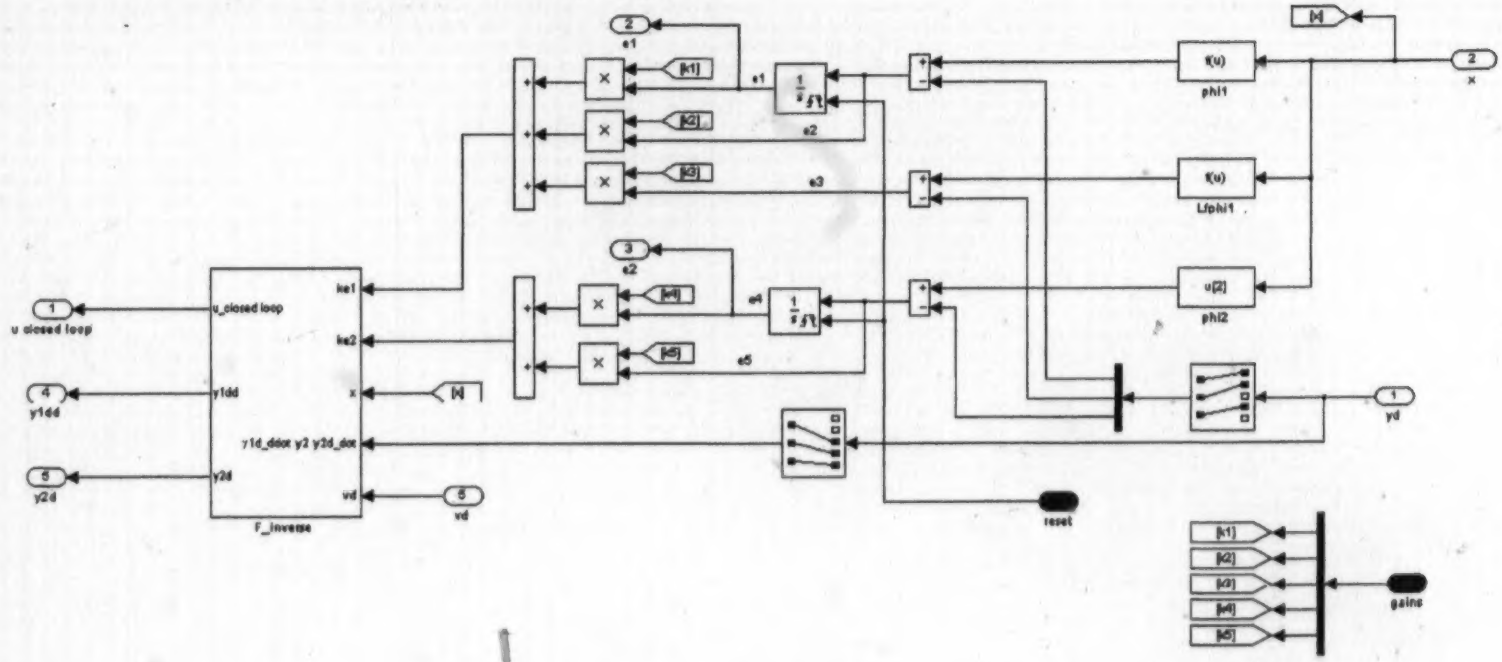

pwm_tune/SM_master/controller
[I_d]
[I_q]
[V_dc]
gains
ma
delta
e1
e2
y1dd
y2d
y1_d
y2_d
reset
vd
fitness control
closed_loop
[ma]
0.4 -> 1
[delta]
-25 -> 25
ma
delta
Ma
Delta
theta_pll
control 1
control 2
control 3
pulse_gen
control signals
-20
I_abc
PLL_en
compensate
PLL_offset
fix
I_PLL
I_d
I_q
I_a
I_b
I_c
new_Ia
new_Ib
new_Ic
I_theta
[I_d]
[I_q]
[I_a]
[I_b]
[I_c]
[newIa]
[newIb]
[newIc]
[I_theta]
Iabc_dq
Data_In
100
[Van]
[Vbc]
van
vbc
Delta_PLL
[delta_pll]
new_PLL
theta_PLL
vd
omega
[V_d]
[omega]
PLL
100
In
avg_out
buffer_average1
fix_dc1
[v_dc]
measure
[e1]
[e2]
[y1_d]
[y2_d]


pwm_tune/SM_master/controller/flatness control
y1d
y2d
yd_3
Trajectory Generator
7
y1_d
8
y2_d
x
gains
reset
vd
Closed Loop Control
3
e1
4
e2
5
y1dd
6
y2d
PWM
1
ma
2
delta

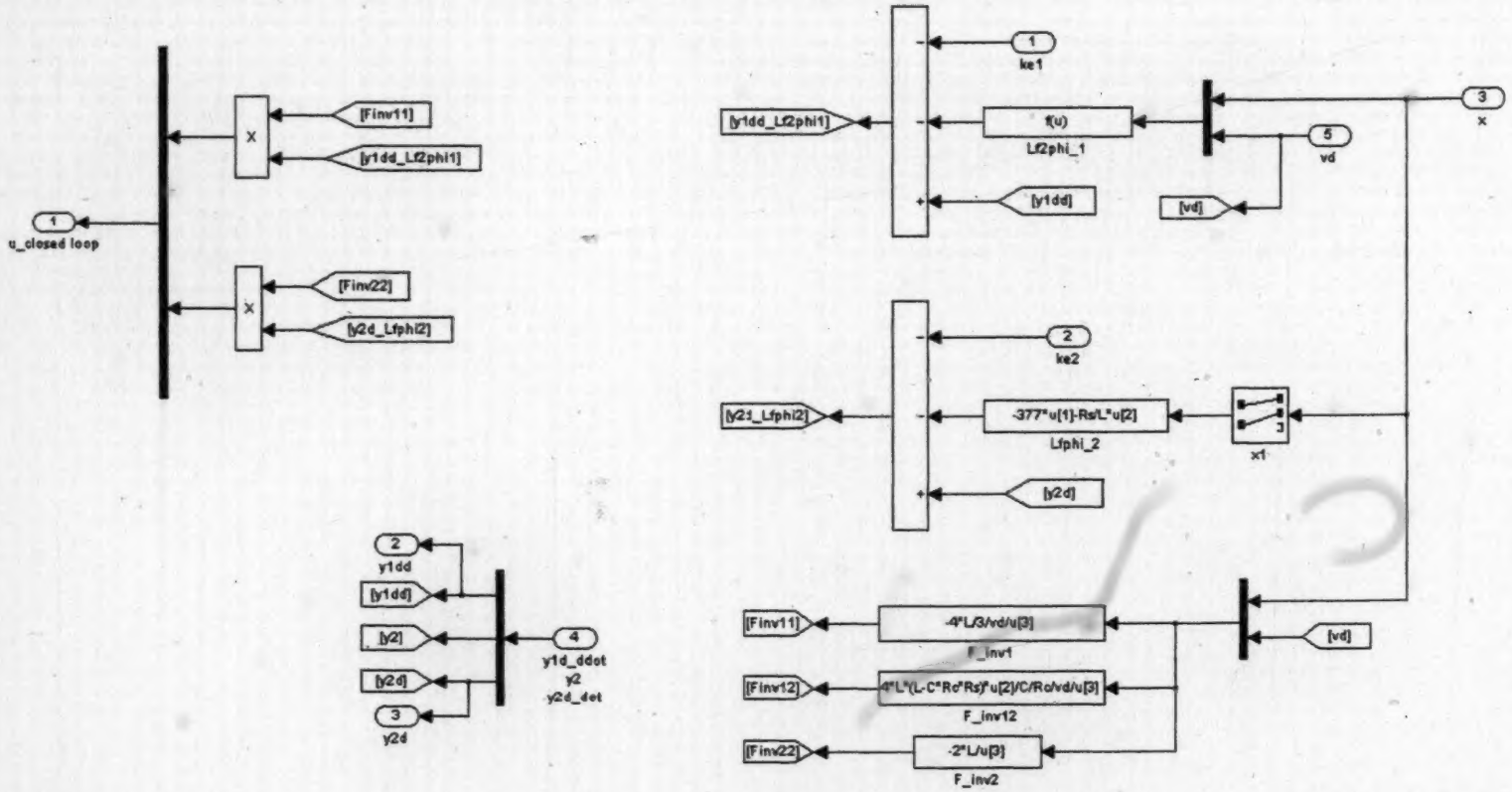
pwm_tune/SM_master/controller/flatness control/Trajectory Generator



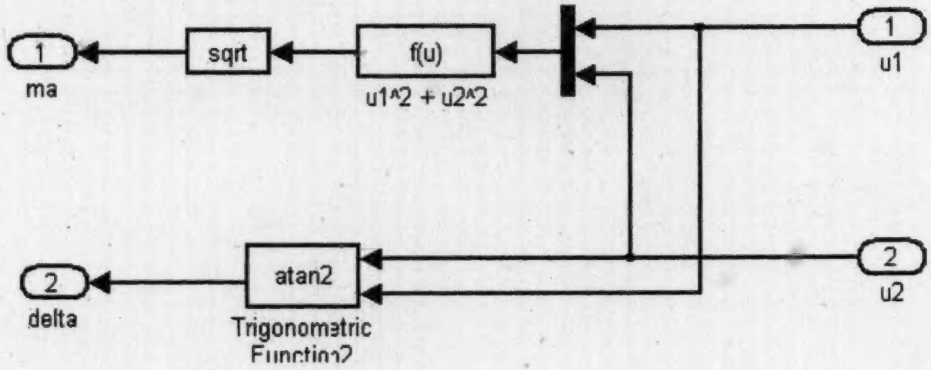
pwm_tune/SM_master/controller/flatness control/Closed Loop Control



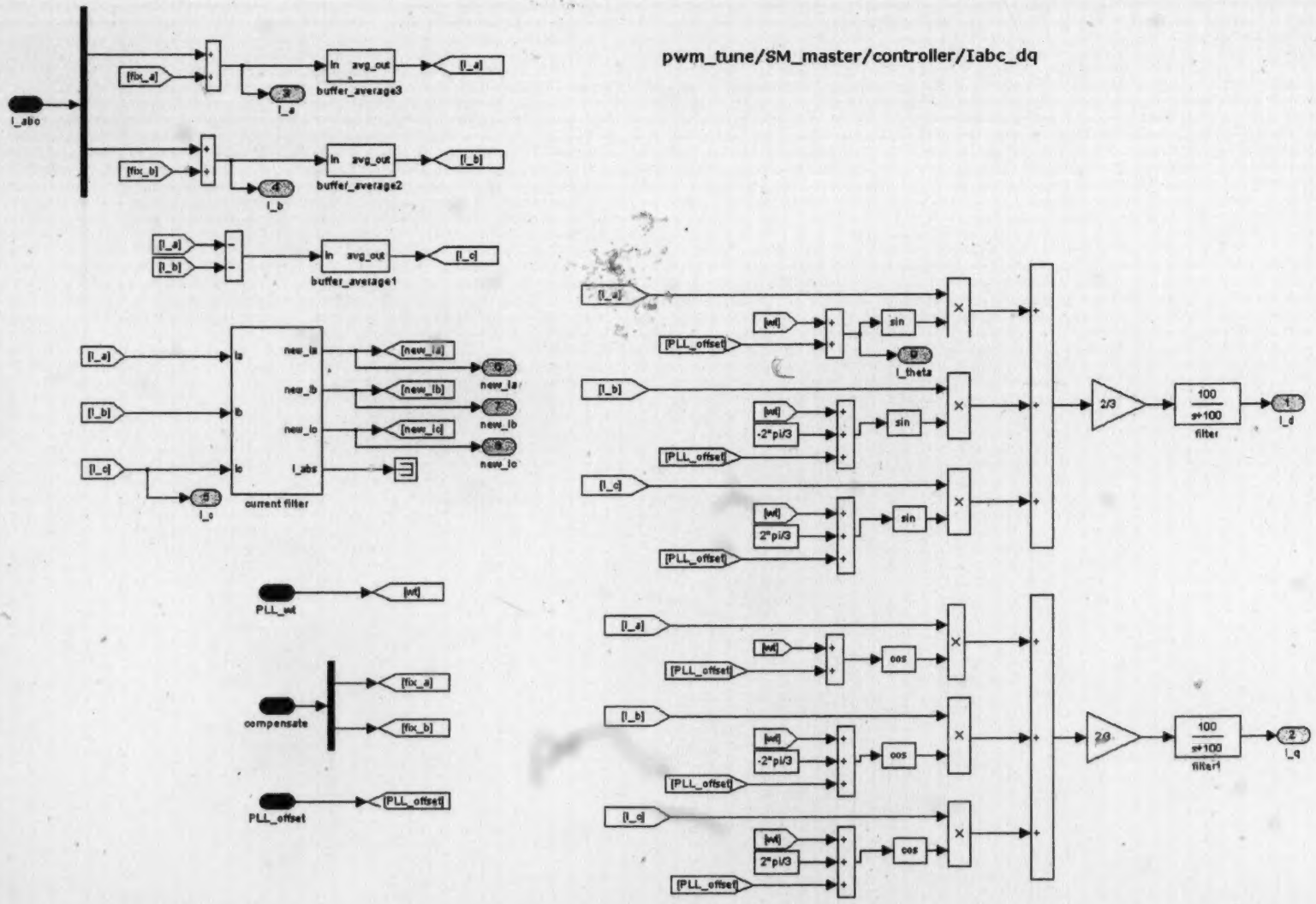
pwm_tune/SM_master/controller/flatness control/Closed Loop Control/F_inverse



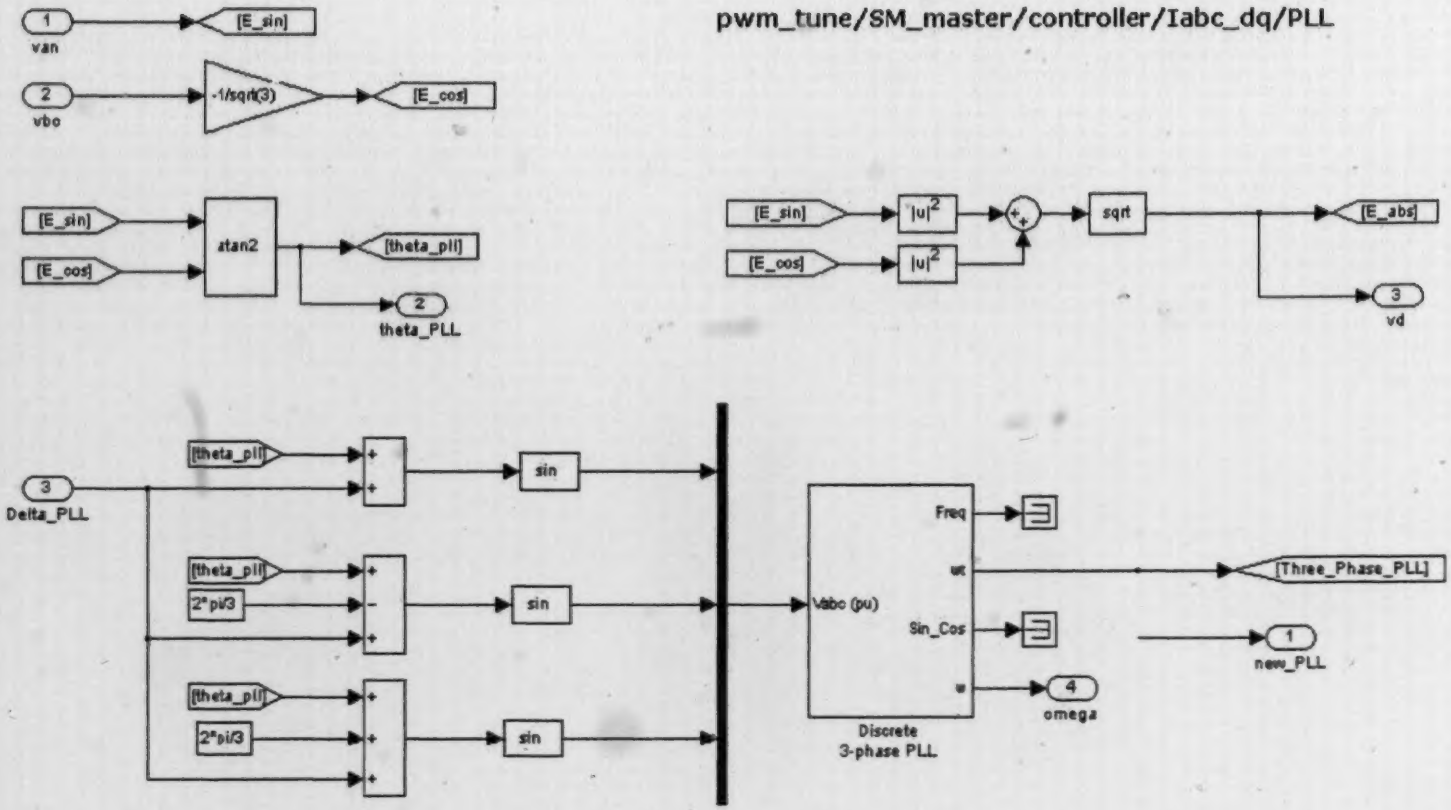
pwm_tune/SM_master/controller/flatness control/PWM/pulse generator



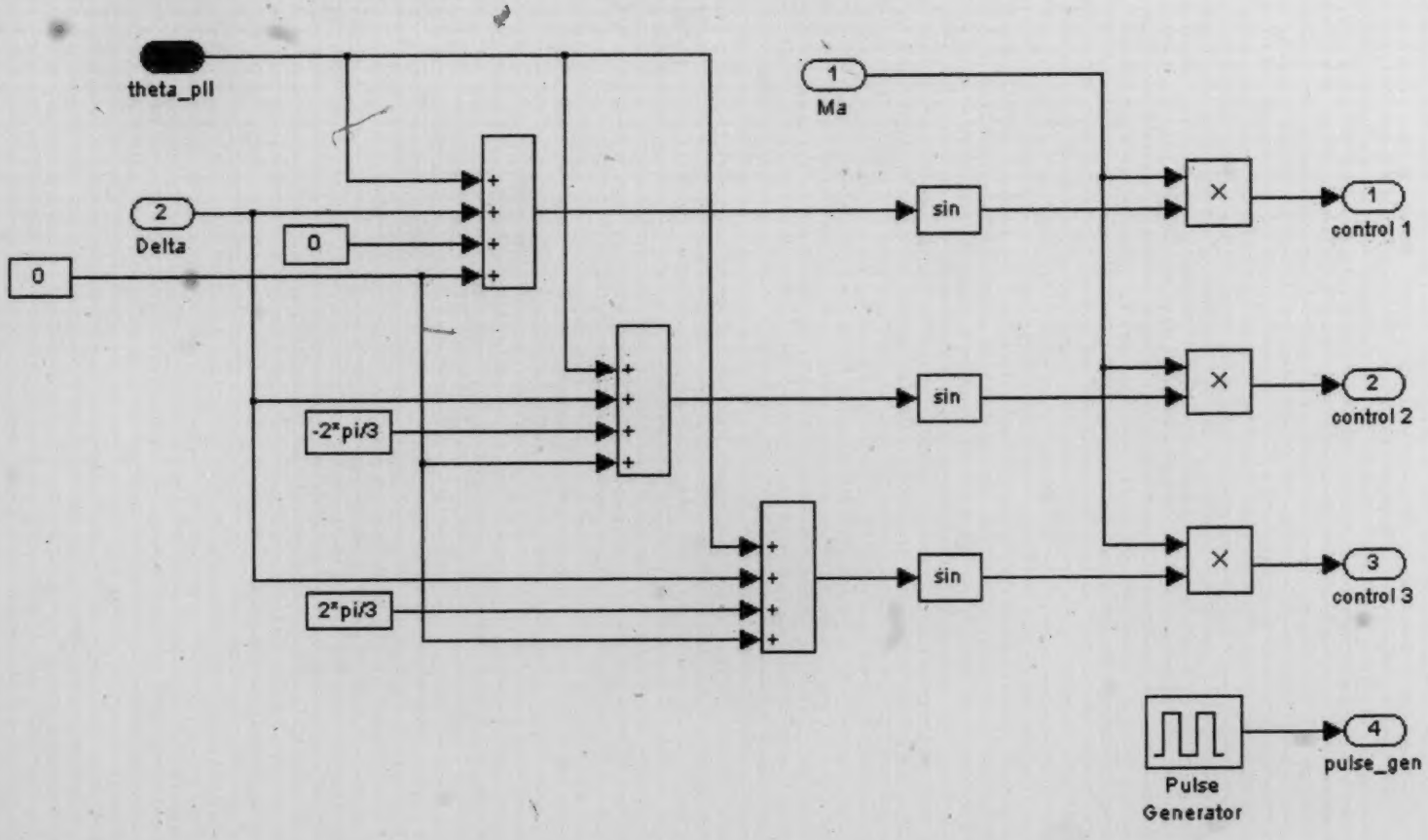
pwm_tune/SM_master/controller/Iabc_dq



pwm_tune/SM_master/controller/Iabc_dq/PLL

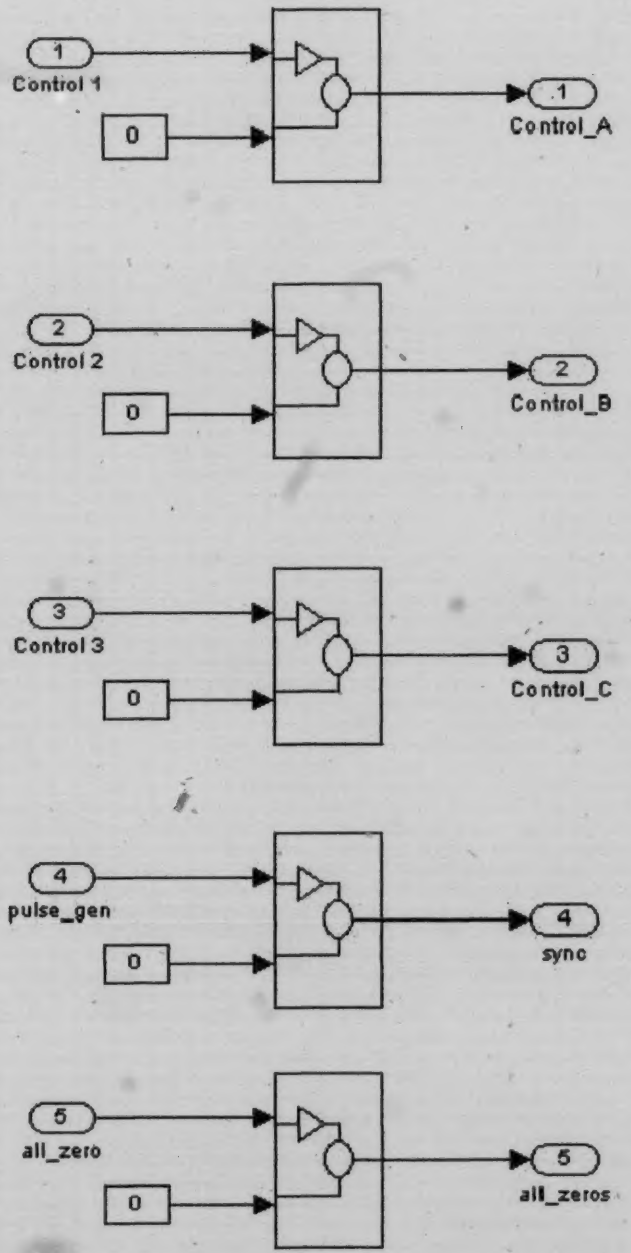


pwm_tune/SM_master/controller/control signals

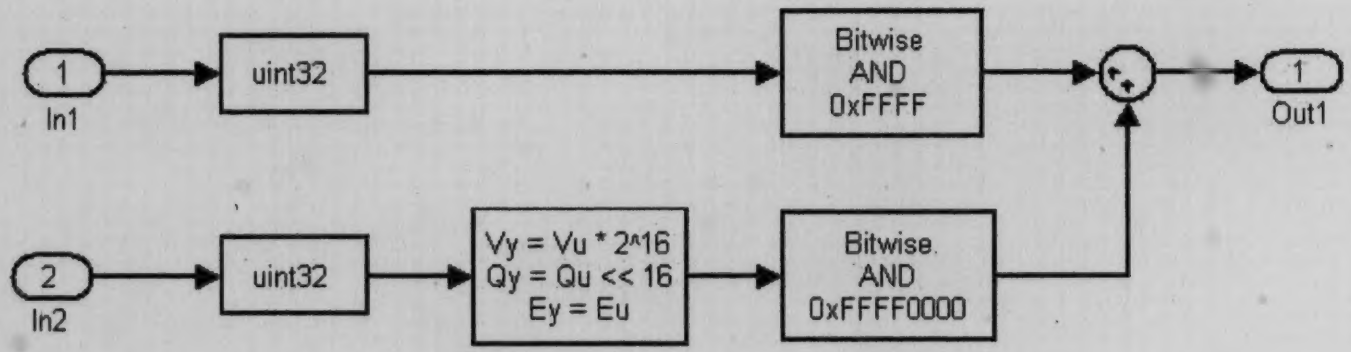


pwm_tune/SM_master/double to uint32 convert

16 bit signal concatenation to 32 bits

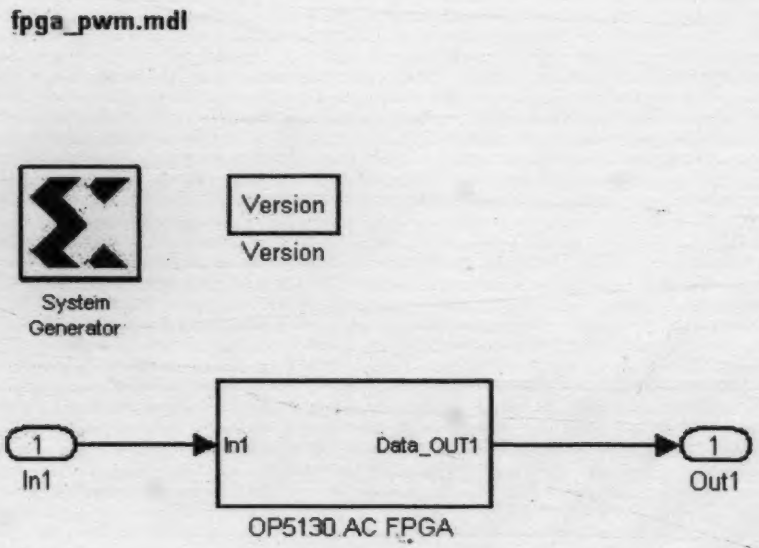


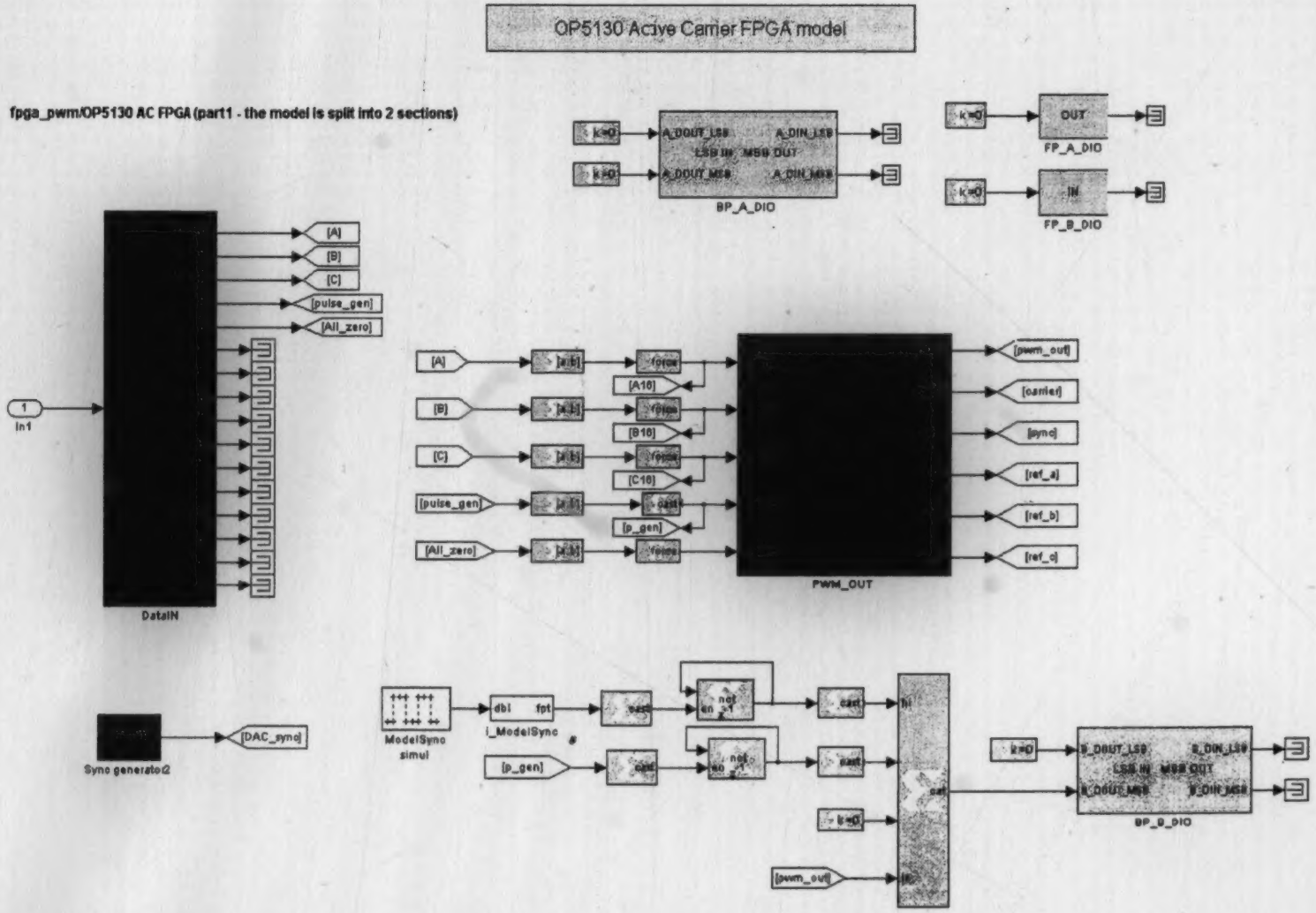
pwm_tune/SM_master/double to uint32 convert/double to 32 bit



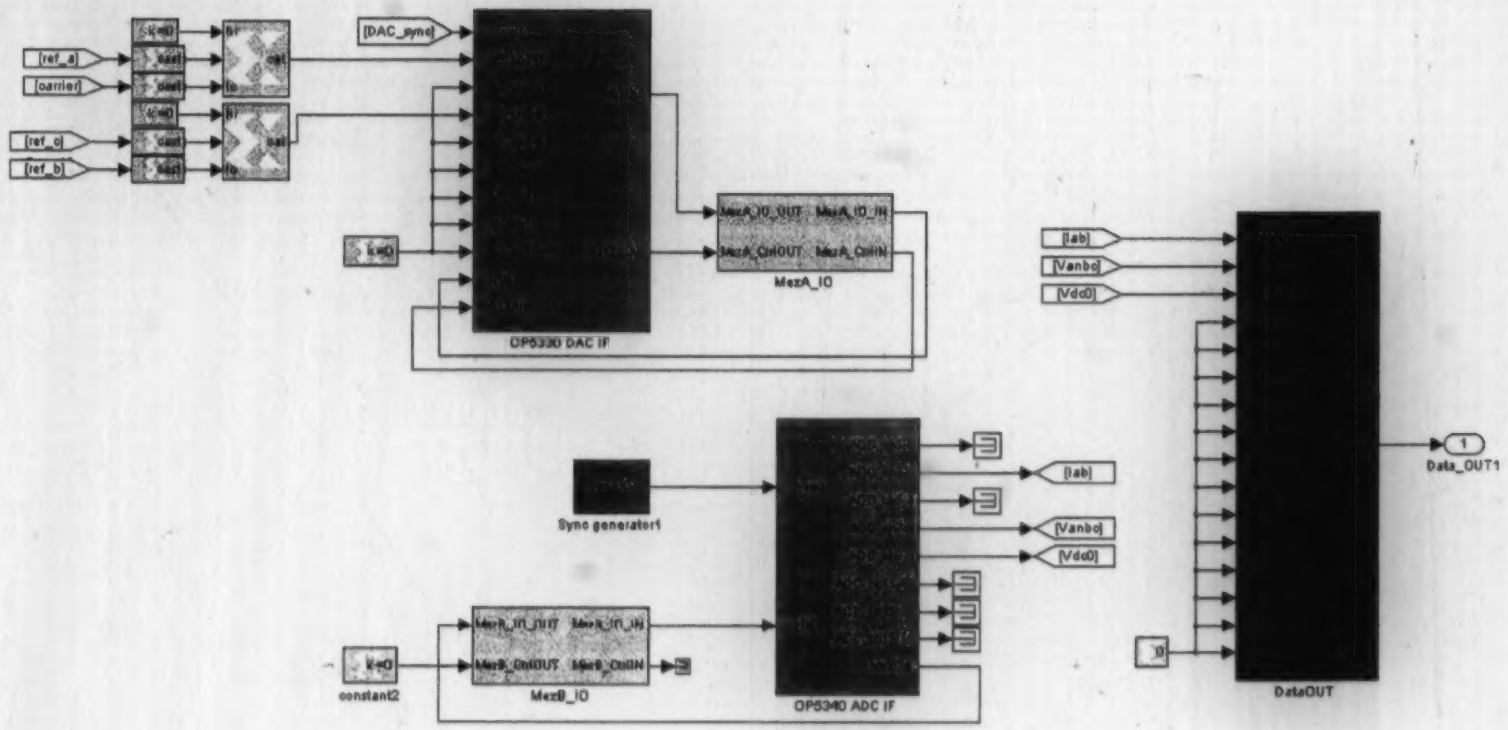
Appendix D

Xilinx System Generator model

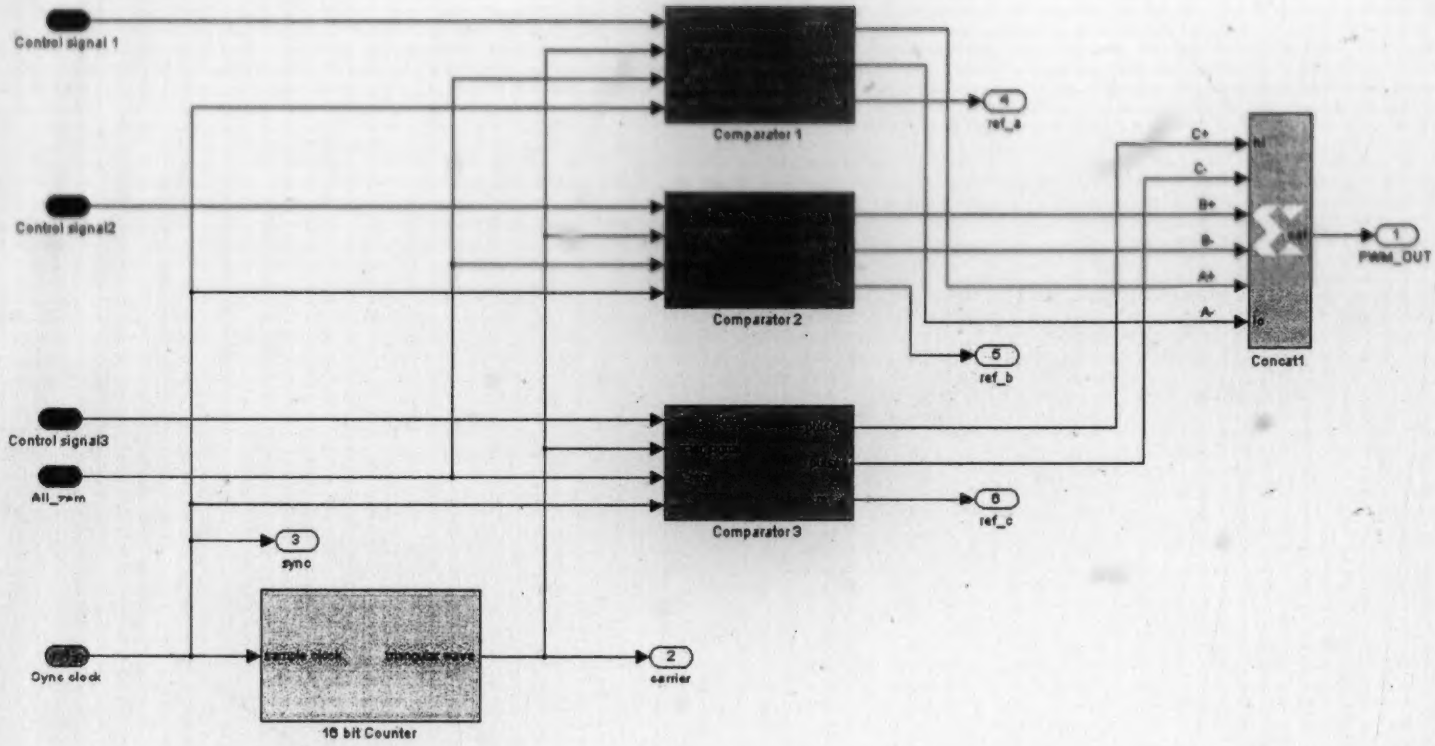



OP5130 Active Carrier FPGA model
fpga_pwm/OP5130 AC FPGA (part1 - the model is split into 2 sections)
BP_A_DIO
FP_A_DIO
FP_B_DIO
DataIN
In1
[A]
[B]
[C]
[pulse_gen]
[All_zero]
PWM_OUT
[pwm_out]
[carrier]
[sync]
[ref_a]
[ref_b]
[ref_c]
[A16]
[B16]
[C16]
[p_gen]
Sync generator2
[DAC_sync]
ModelSync simul
i_ModelSync
BP_B_DIO

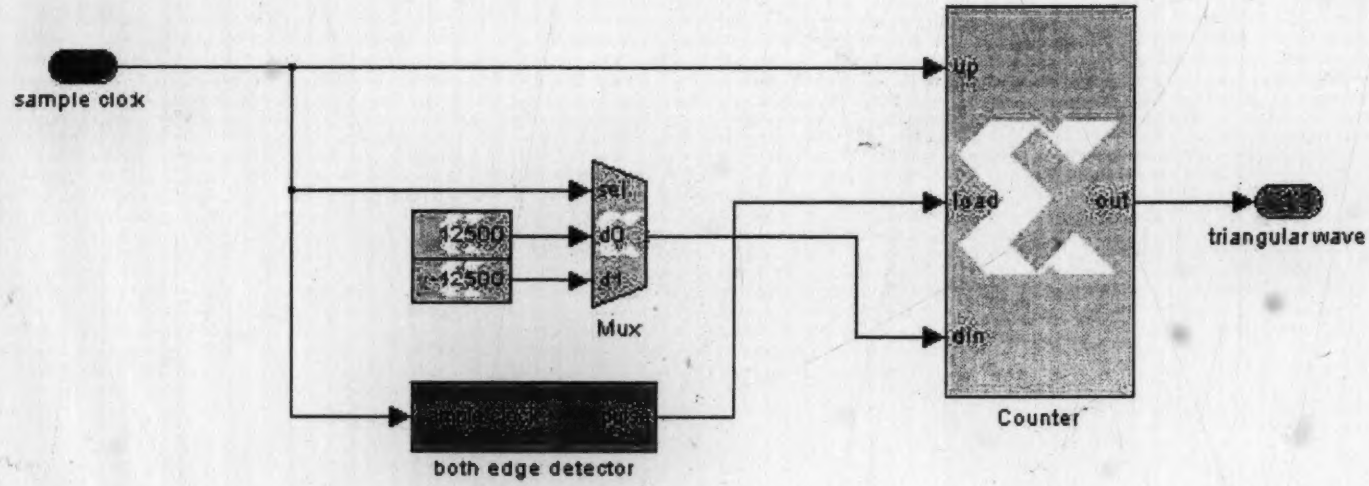
fpga_pwm/OP5130 AC FPGA (part2)



fpga_pwm/OP5130 AC FPGA/PWM_OUT/Synchronized PWM



fpga_pwm/OP5130 AC FPGA/PWM_OUT/Synchronized PWM/16 bit Counter



fpga_pwm/OP5130 AC FPGA/PWM_OUT/Synchronized PWM/Comparator 1